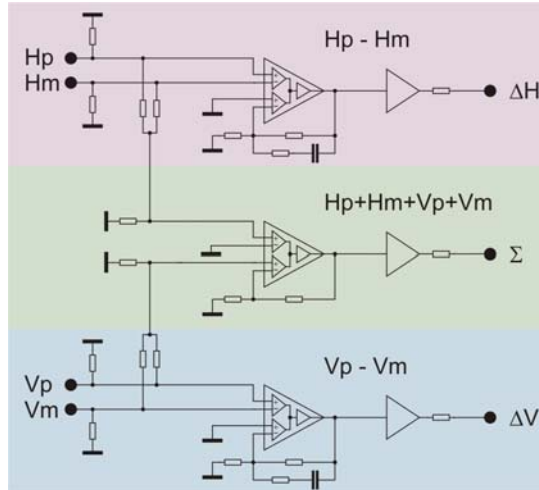


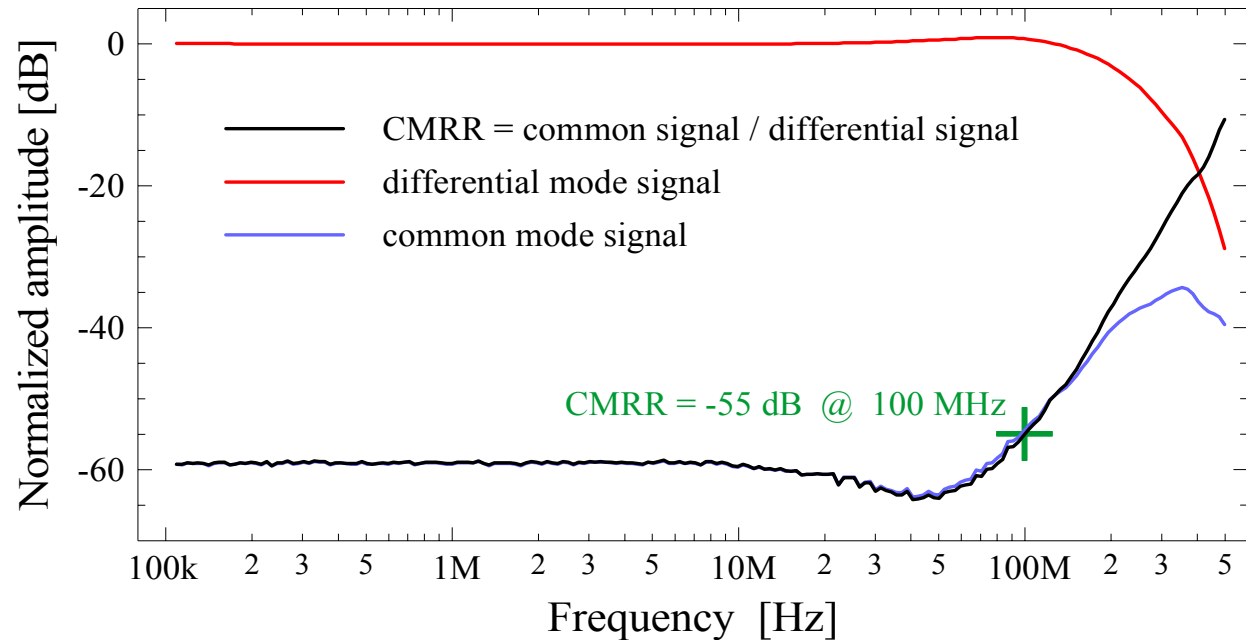
(Beam Diagnostics) Data Acquisition

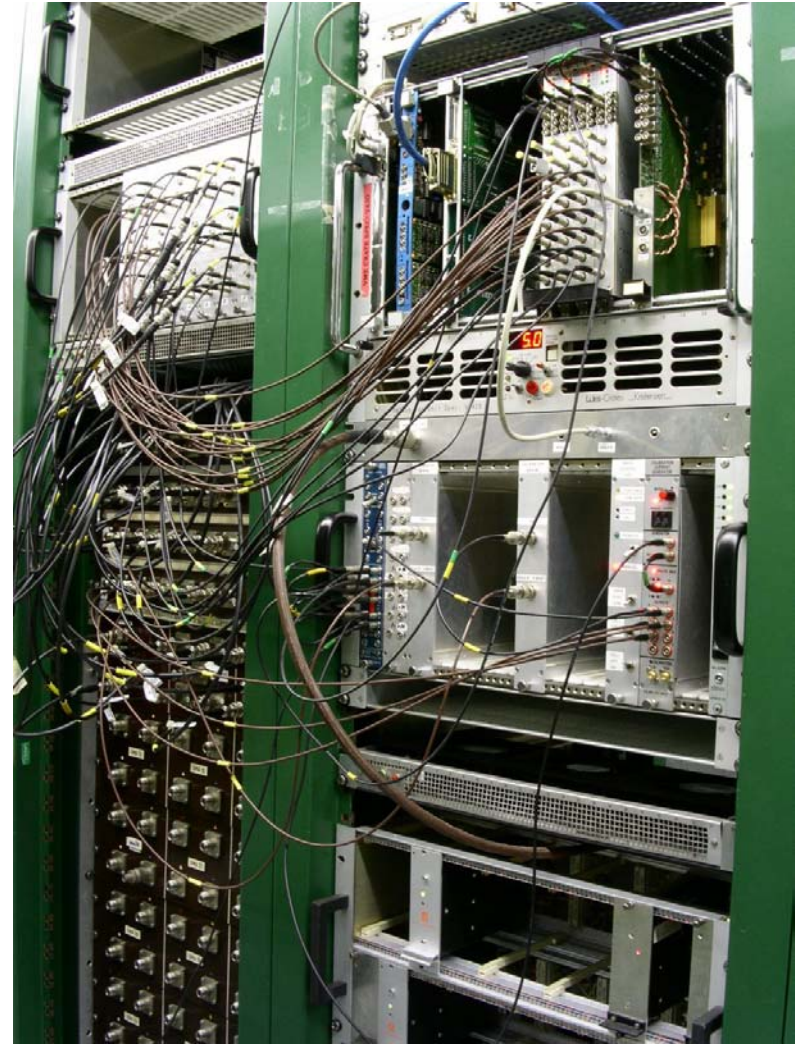
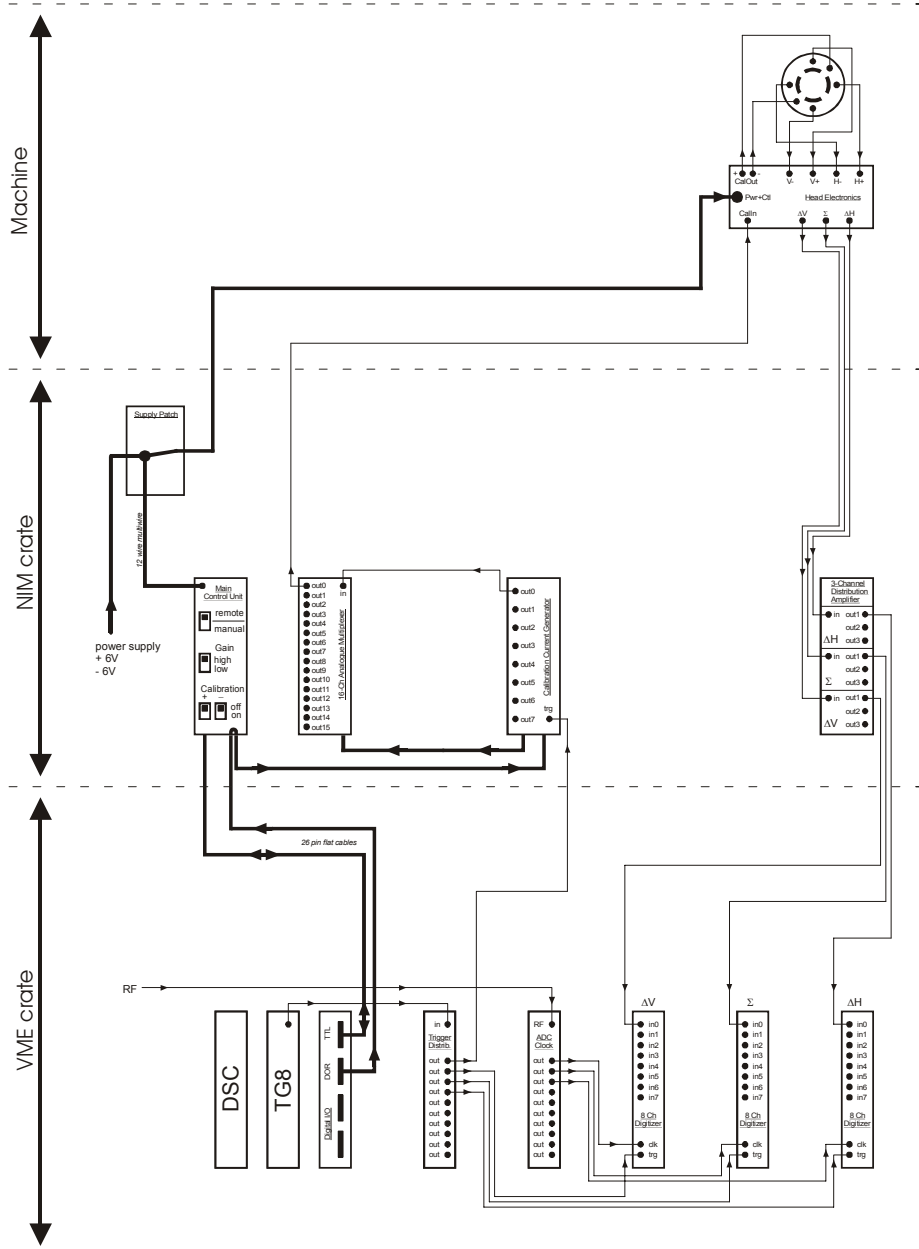
Marek GASIOR, CERN, AB/BDI
email: marek.gasior@cern.ch

- BPM system layout
 - System components
 - Testing & Calibrating
 - ADC modules

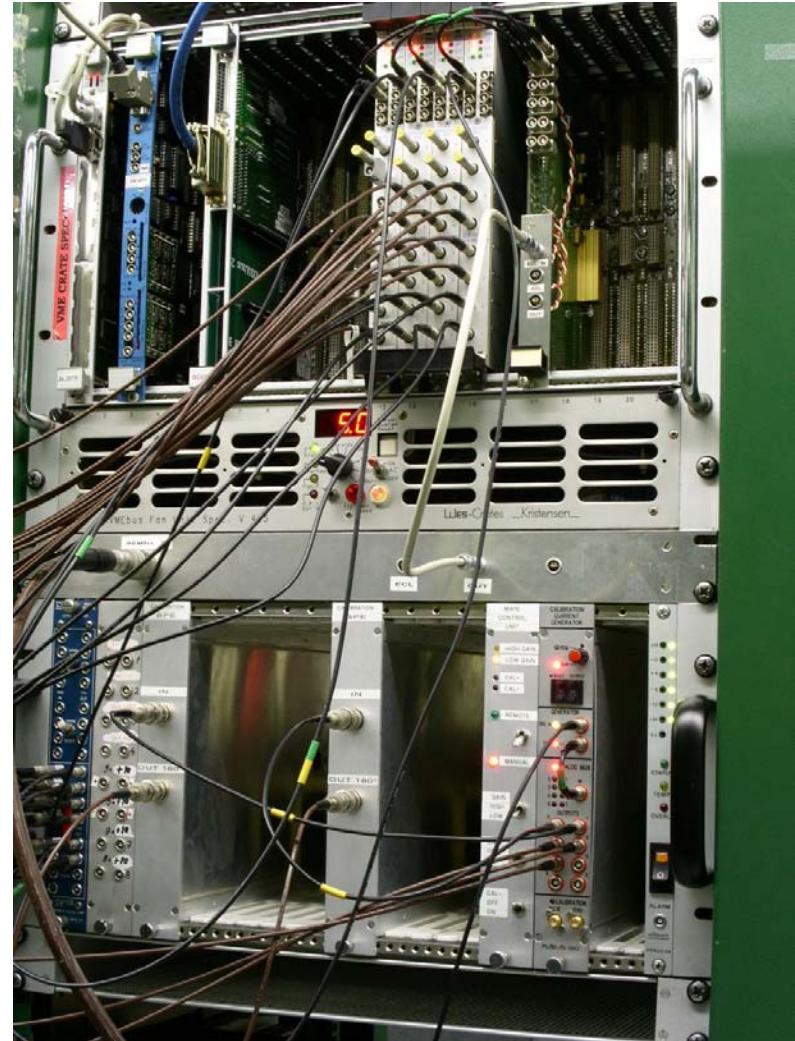
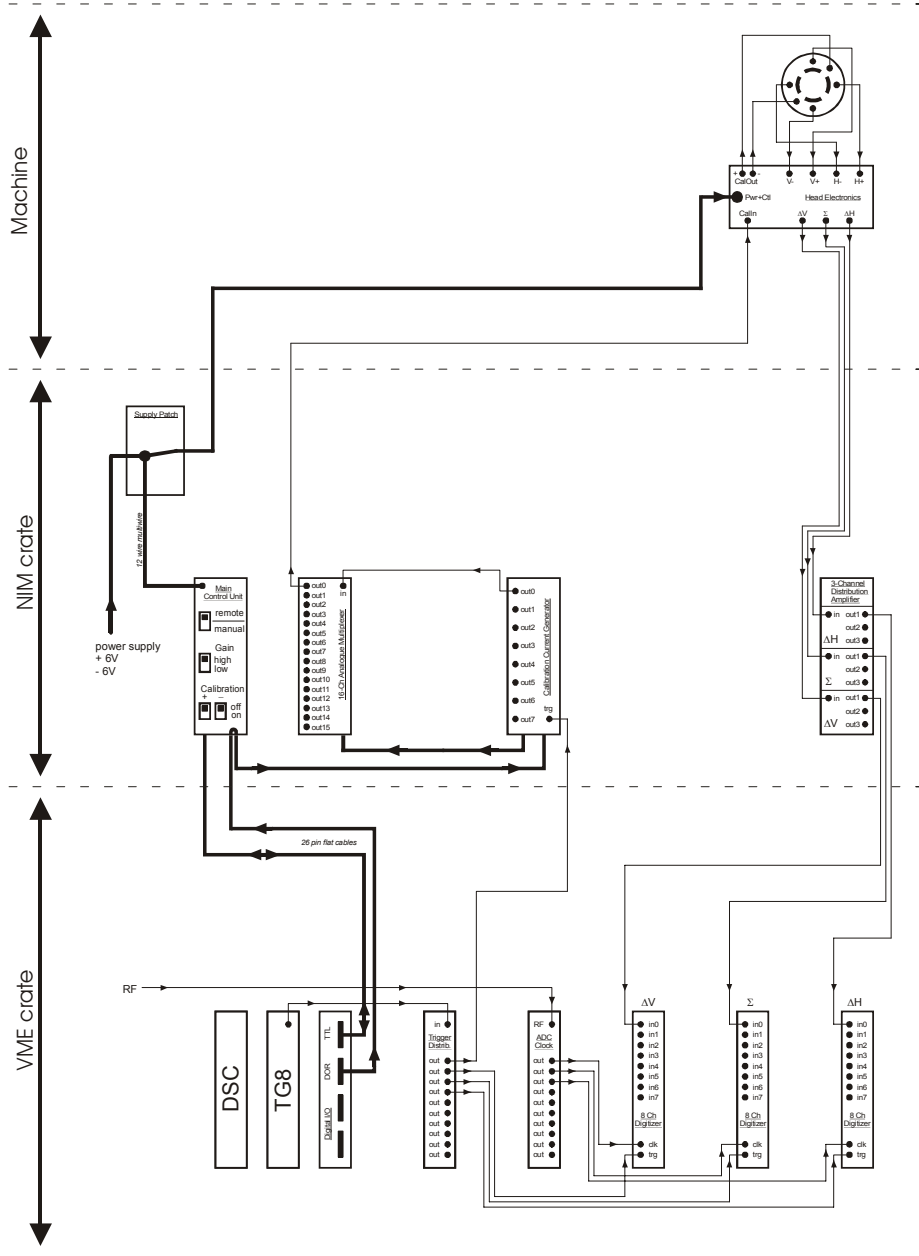


- The module produces Δ and Σ signals
- Δ high cut-off frequency is about 200 MHz, for Σ signal - 250 MHz
- The CMRR at 100 MHz is as high as 55 dB
- Δ signal cable lengths have to be matched within 1.6 ps, (i.e. within some 0.3 mm) to have deterioration of the CMRR from their length difference below -60 dB at 100 MHz
- Once the Δ signals are made, it is enough to have the long cables going to the equipment room matched within 0.5 ns (a factor of 300 less than for the cables pick-up - hybrid)

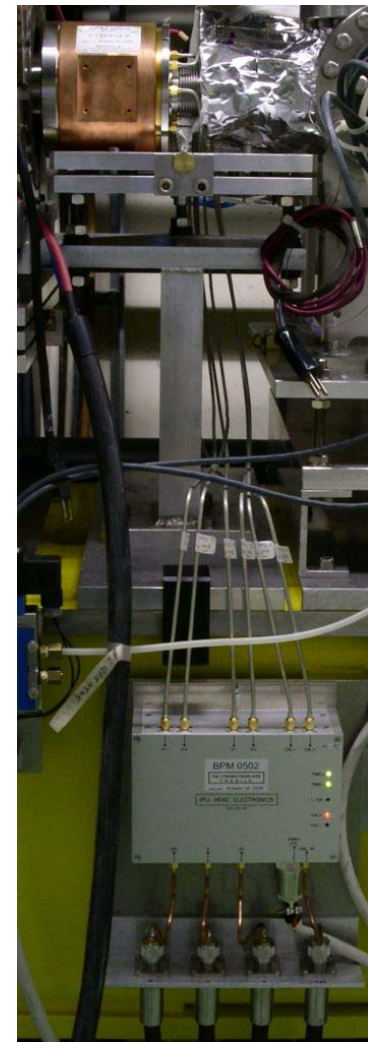
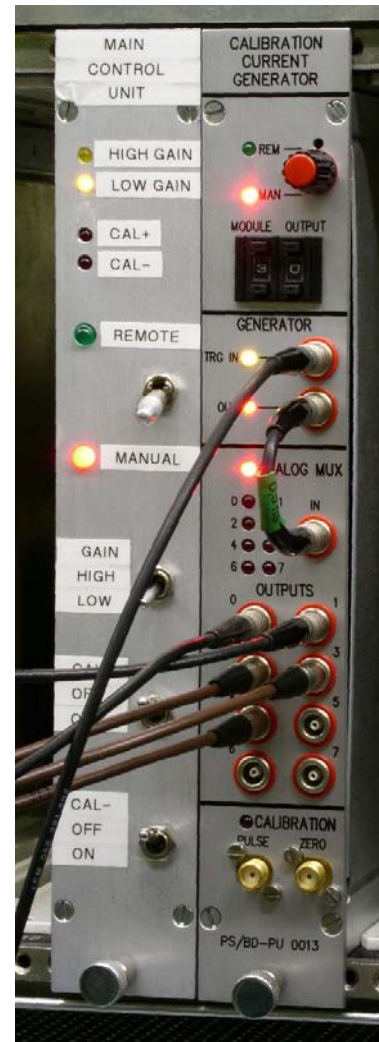
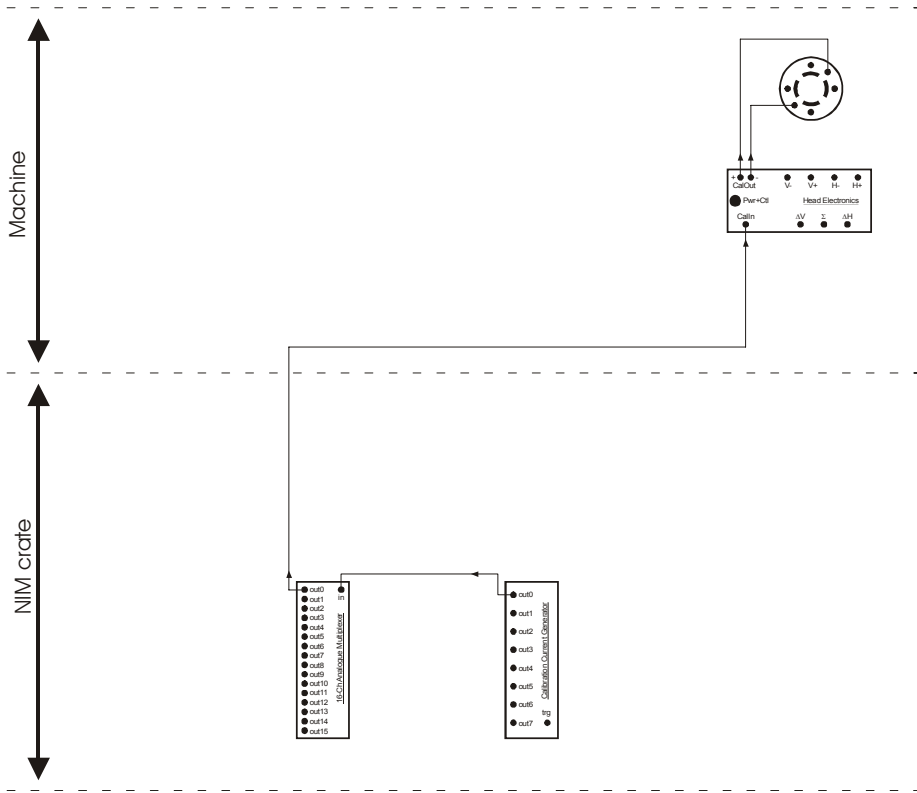




- Reception Patch
- Distribution Amplifiers
- ADC modules
- The system is modular



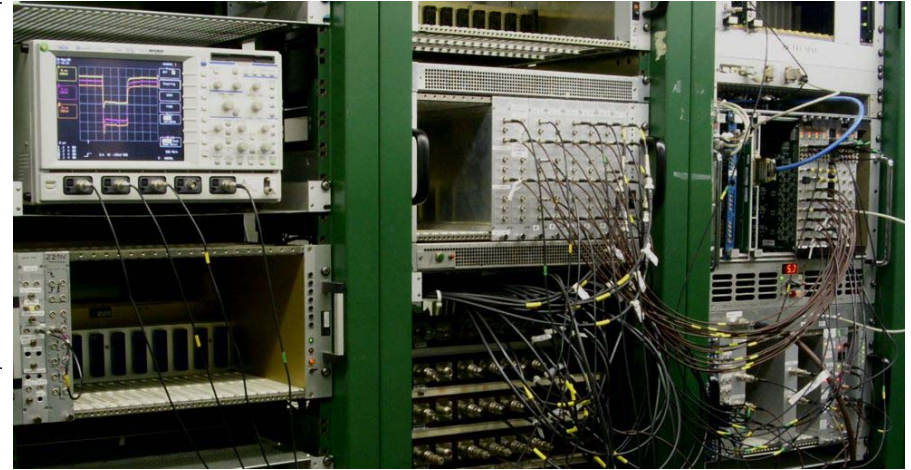
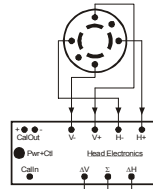
- DSC Host
- TG8
- Clock Distribution
- Trigger Distribution
- Calibration Current Generator
- Main Control Module
- I/O Modules



- All system channels can be tested, also in parallel with the standard beam operation
- The CCG is used to calibrate the pick-ups for the beam intensity measurement
- There is only one CCG for all pick-ups to have always EXACTLY the same pulse amplitude, the pulses are switched by analogue multiplexers

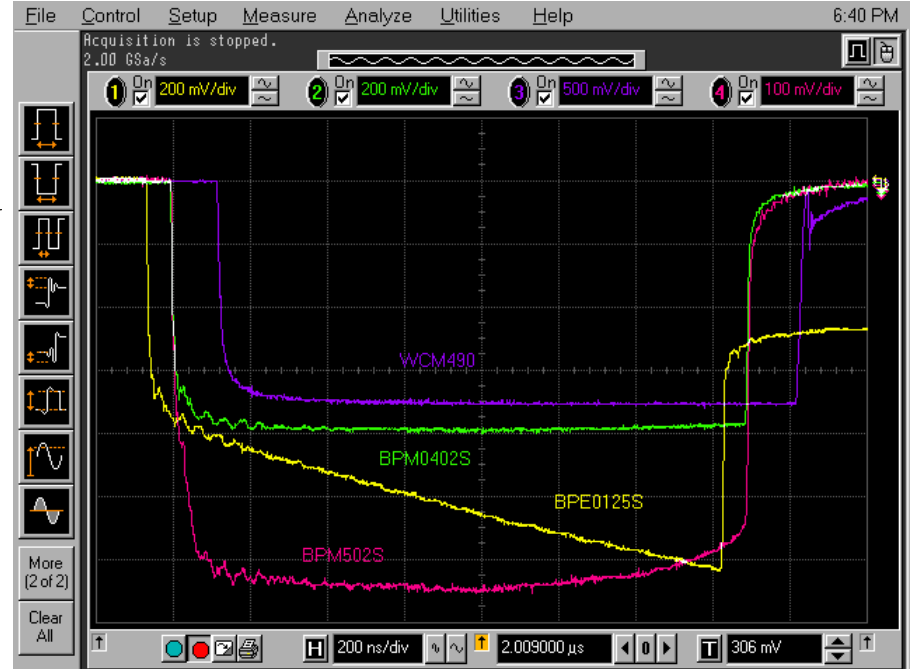
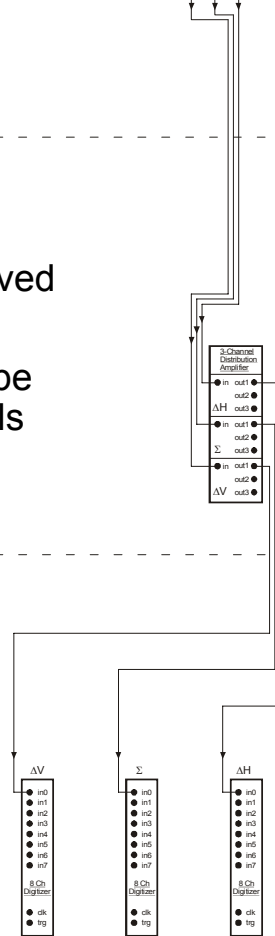
- The Calibration Current Generator (CCG) delivers current pulses of $300 \text{ mA} \pm 0.1\%$
- The pulse length is $1.5 \mu\text{s}$ (testing) and $150 \mu\text{s}$ (for calibration to reveal the pick-up signal droops)

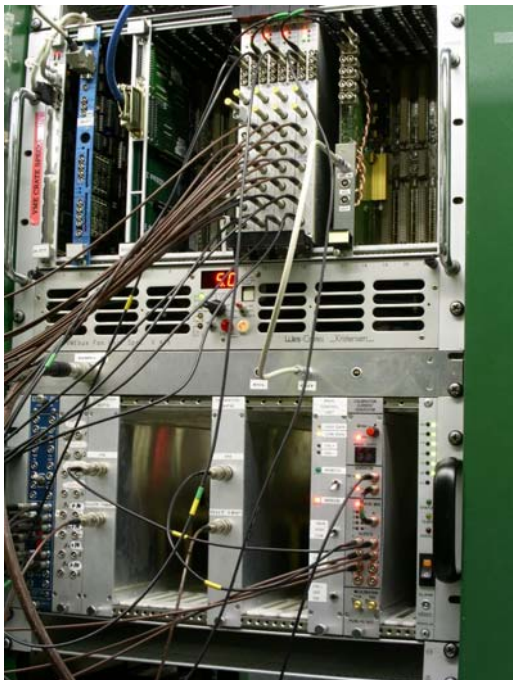
Machine



- All analogue signals can be observed on a scope in the equipment room
- Beam positions and currents can be easily calculated from these signals

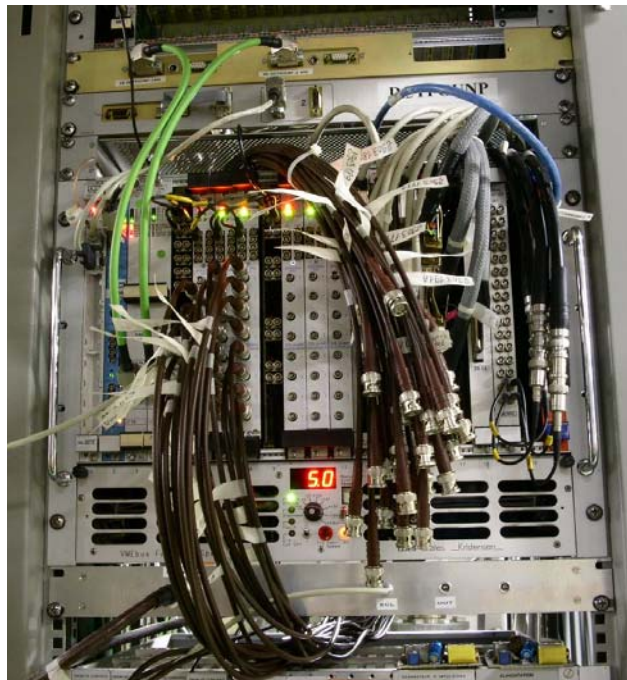
VME crate



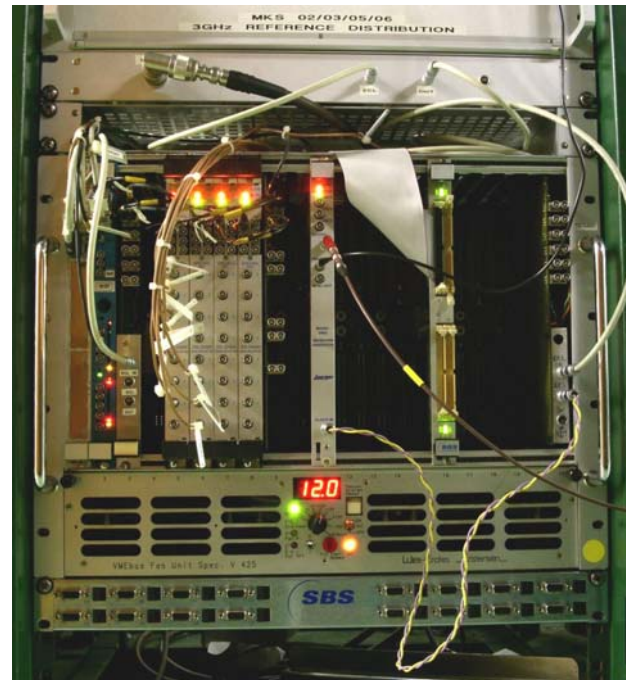


BPEs, BPMs, BPRs, WCMs

- ADC modules are of the same type for all instrumentation equipments
- Standard acquisition crate contains:
 - host
 - TG8 timing module
 - ADC modules
 - ADC clock distribution
 - ADC trigger distribution

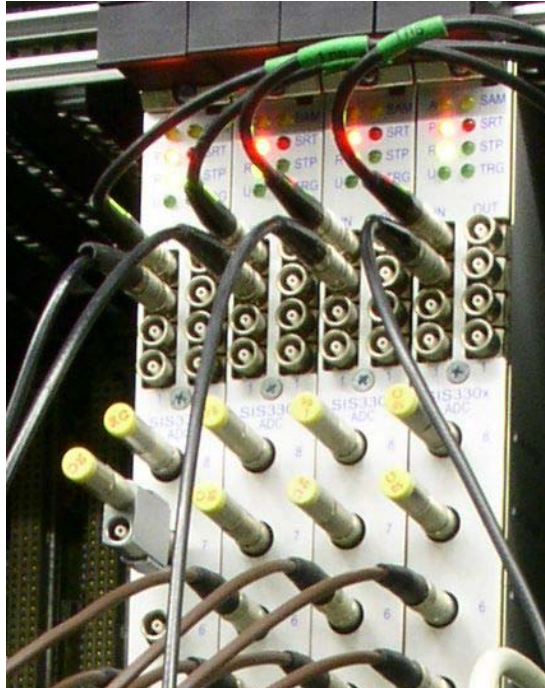


SEM-grids

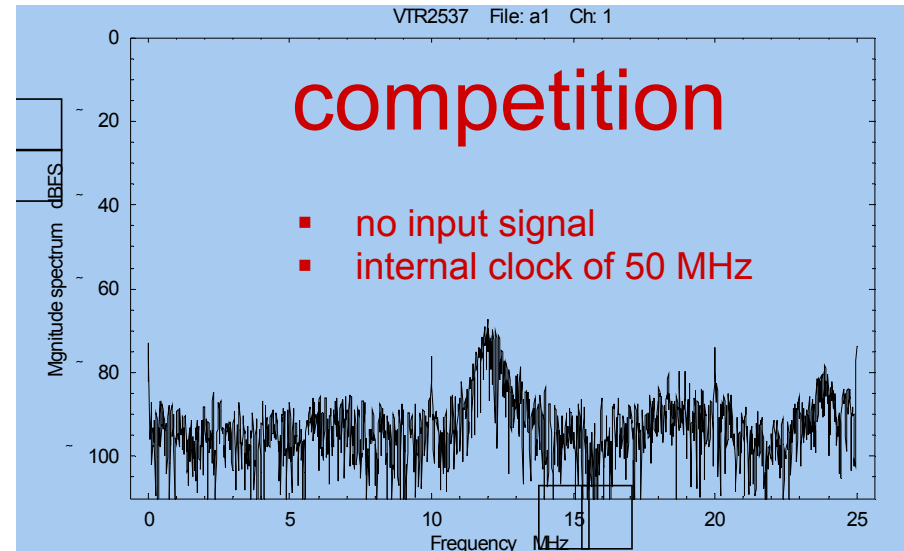
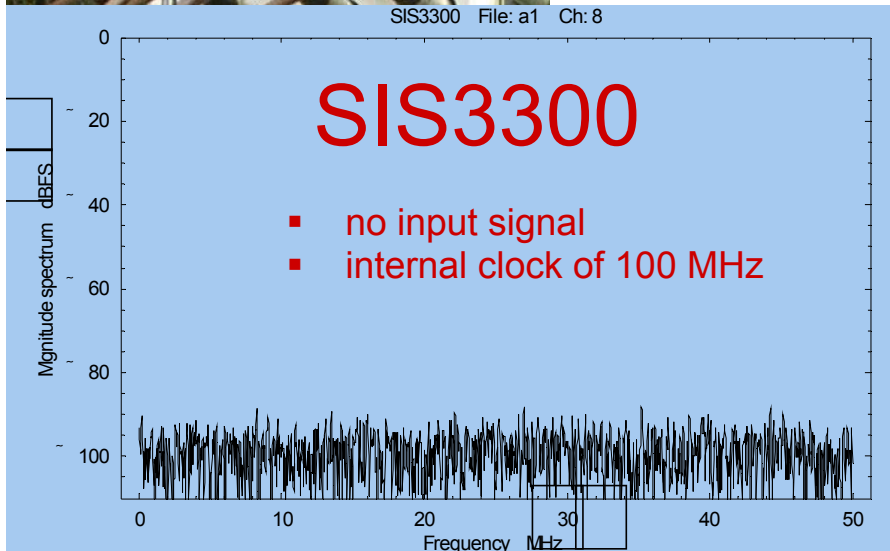


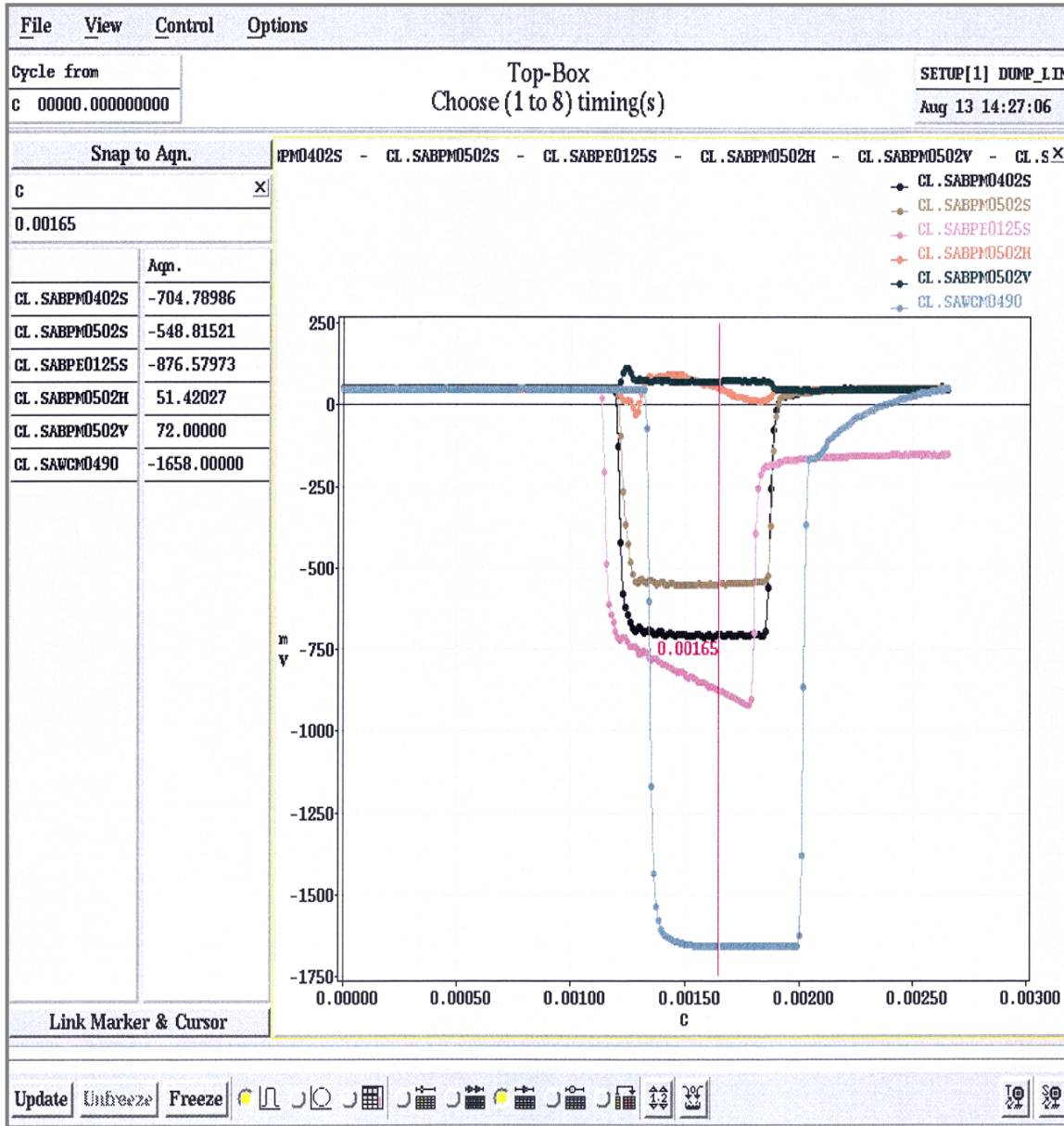
RF Equipment

- All ADCs work with the same clock of 96 MHz (5×19.2) derived from the RF
- Each sub-system has its own trigger
- Within one sub-system all ADC modules use one trigger
- The ADC clock and trigger inputs have 50Ω impedance, so the signals are actively distributed to all modules



- 12-bit, 100 MHz, 8 channel
- Memory: 256 k samples / channel
- Each module starts acquisitions a programmed number of clock ticks after the hardware trigger and stops automatically after the desired number of samples is stored
- Multi-event operation is used: a certain number of events is stored in the memory one after the other (in our case each beam pulse) and transferred at the end of the cycle (cycles of 1.2 s)
- The modules run in the dual bank memory scheme: new data is acquired (to memory bank A) while data from the previous cycle is being transferred (from memory bank B)
- The modules have many other nice things (as averaging, special trigger modes) which we do not use (for the time being)
- The modules have very good noise / interference performance





Σ BPE 125

Σ BPM 402

Σ BPM 502

WCM 0490

ΔH BPM 502

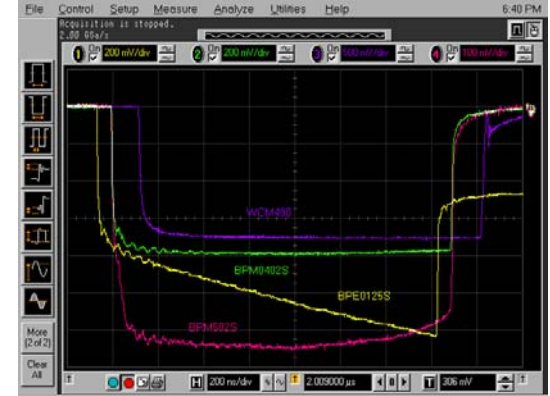
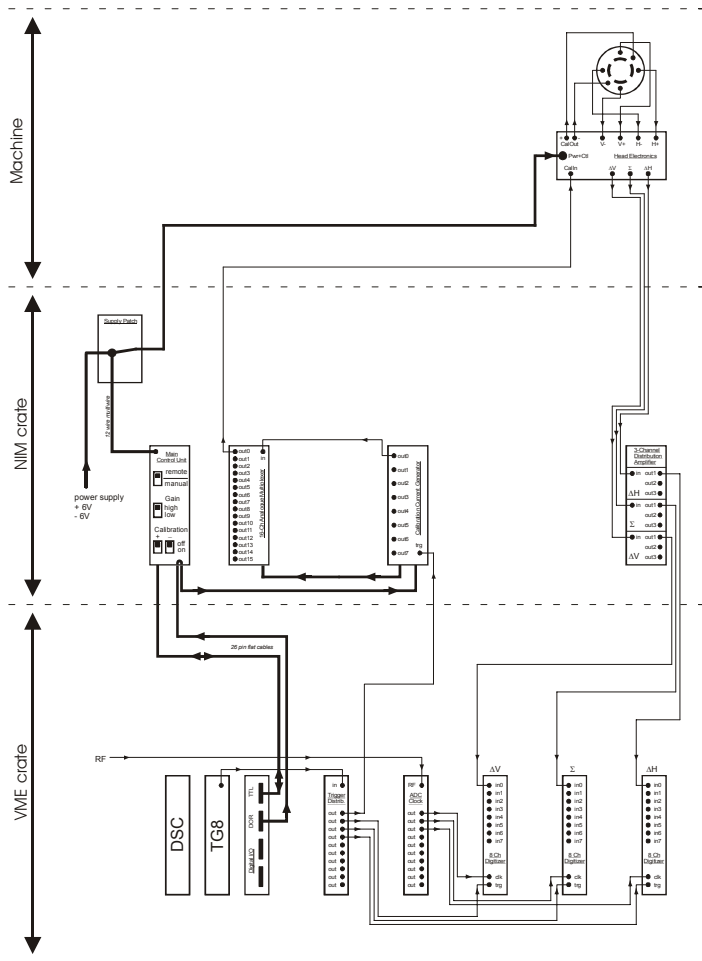
ΔV BPM 502

So far:

- ADC samples were displayed as on a digital scope
- The software is being developed to deliver more complete data

In the future:

- The signals will be displayed in mm, A, etc.
- Integration within a given window to calculate the charge
- Beam position in mm, beam current in A, measurements in a table and on a graph
- Calibration automated



- The beam diagnostic data acquisition was successfully used to commission the machine
- Simplicity and flexibility were very important
- Scope observation was very useful
- Testing and calibration capabilities were much appreciated (by the operation as well as the HW specialists)
- In the future the system modularity will be beneficial
- The system software will still be developed

Ups...

