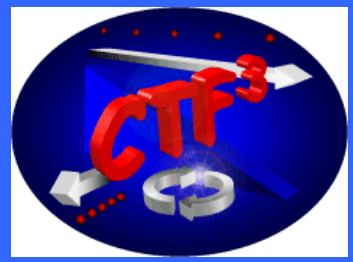
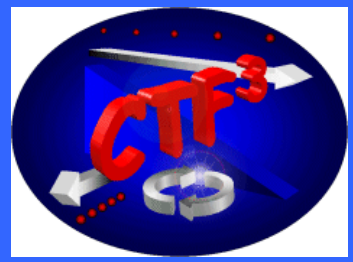
KICKERS FOR CTF3 & CLIC

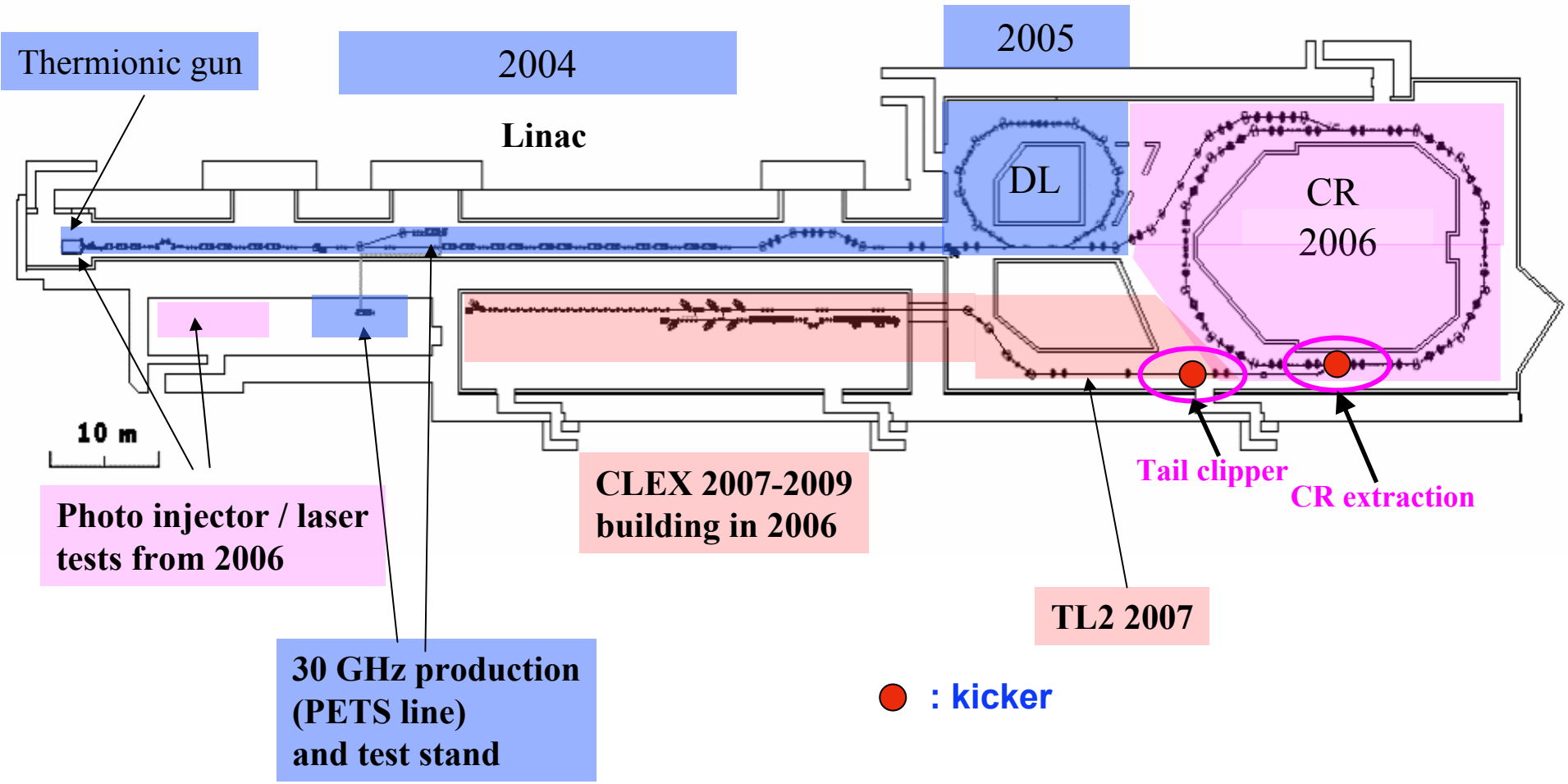


Michael Barnes
CERN
AB/BT

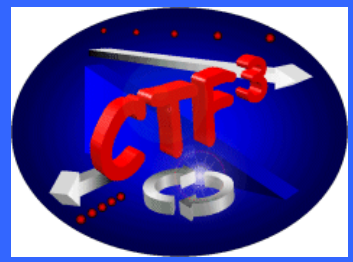
Prepared with input
from
Tony Fowler

CTF3 Programme





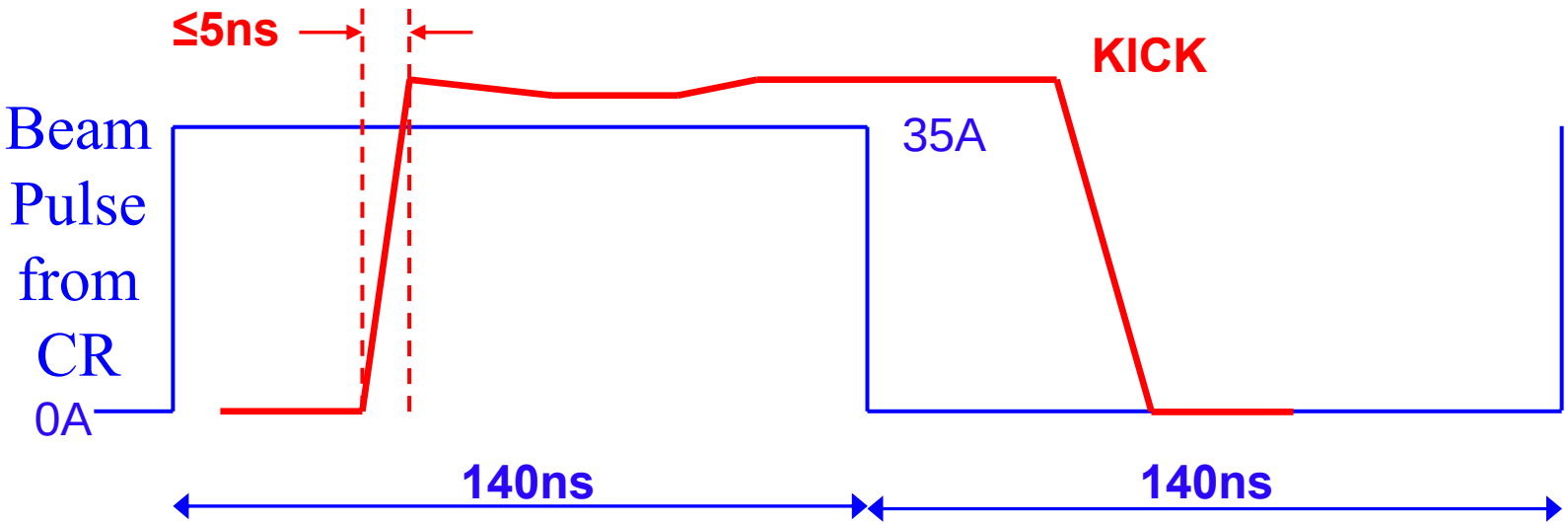
CTF3 & CLIC Strip-Line Kickers



- **Strip-line kickers: preliminary specifications**

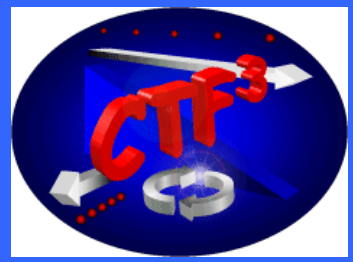
		CR Extraction	CLIC	Tail Clipper	
Beam energy		300	2500	200	MeV
Total kick deflection angle ("B" & "E" Fields)		5	2.5	1.2	mrad
Strip-line plate separation		40	20	40	mm
Strip-line length		1.7	3	Up to 1.5	m
Rise & fall-times (0.25% to 99.75%)		≤ 70	≤ 30	≤ 5 !	ns
Pulse duration		200	50 to 60	Up to 140	ns
Flat-top reproducibility		± 0.1	± 0.1	NA	%
Flat-top stability (including droop)		± 0.25	± 0.25	NA	%
Repetition rate	Initial	5		5	Hz
	Nominal	50	150	50	Hz
Pulse voltage		9	10.5	3.2 for 1m	kV
Pulse current (into 50 Ω load)		180	210	64	A
Timing Jitter				≤ 1 rms	ns

Tail Clipper: Introduction



- Output from CTF3 CR is 140ns long (35A beam current);
- Kicker is required to be able to adjust length of beam pulse;
- Maximum duration of required kick pulse is 140ns;
- Fast rise of kick pulse is required to minimize uncontrolled beam loss;
- "Flat-top" of kick pulse is not important as deflected beam is to be thrown away.

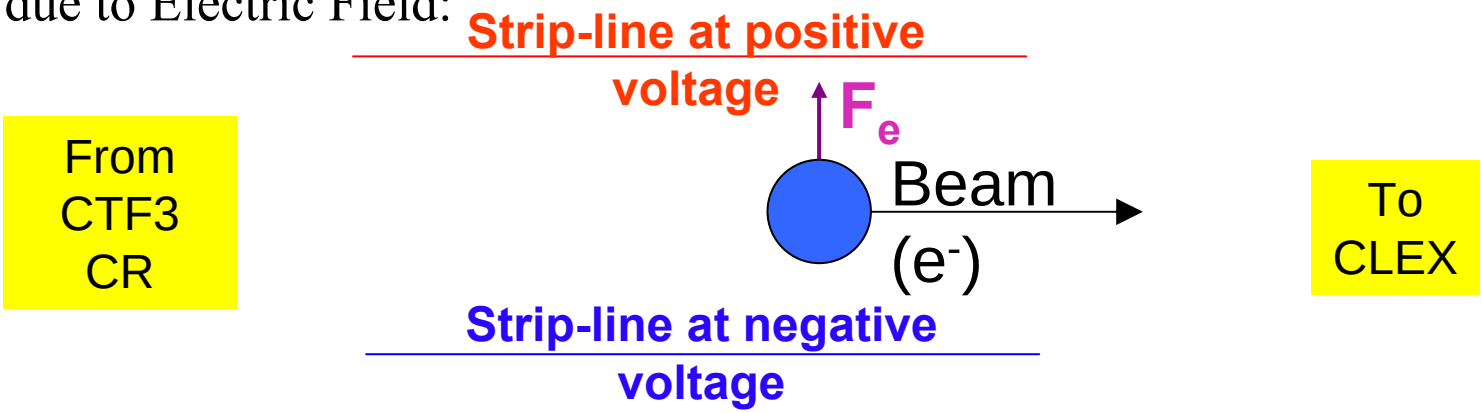
Tail Clipper: Rise Time



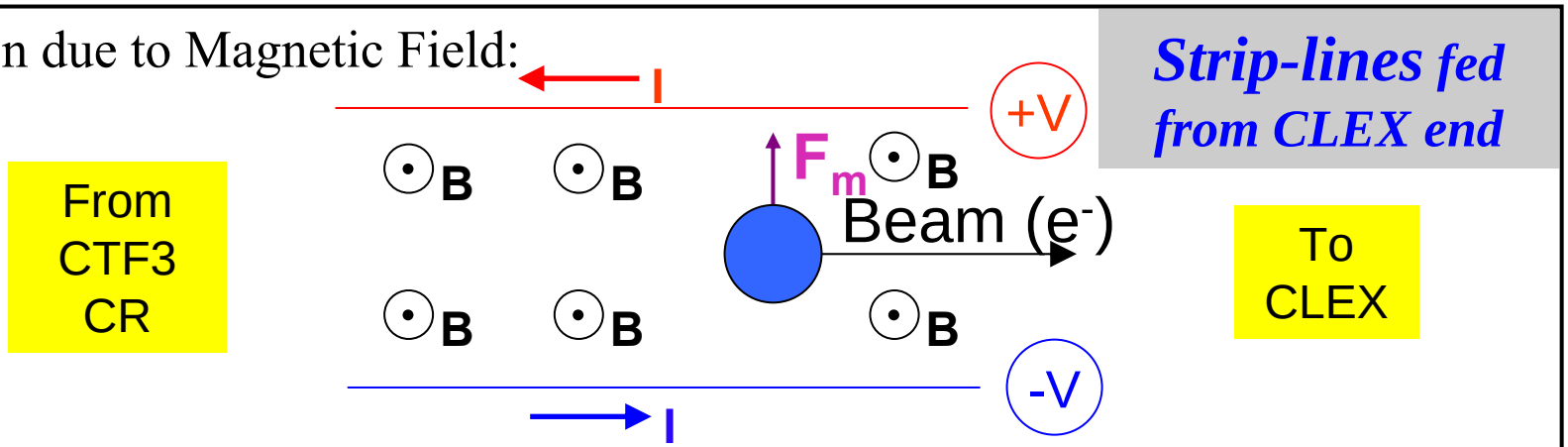
- Tail Clipper requires short rise-time ($\leq$ 5 ns) !.
- To provide 1.2 mrad, with strip-lines terminated in 50 Ω, requires 3.2 kV on 1 m long strip-lines;
- Electrical pulse propagating through 1m strip-lines, at speed of light, takes 3.3 ns!
- In order that CTF3 beam does not "see" fill-time of strip-lines can the strip-lines be "charged" from the CR (beam entrance) end ?

Tail Clipper: Deflection

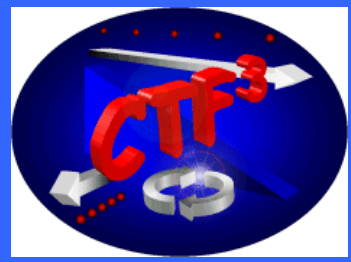
Deflection due to Electric Field:



Deflection due to Magnetic Field:



Tail Clipper: Conclusions



- To make use of both the electrical and magnetic fields to deflect the beam, the strip-lines must “charged” from the CLEX (beam exit) end.
- In order that plate fill time does not significantly effect deflection rise time, several sets of strip-lines, mechanically in series, will probably be required.

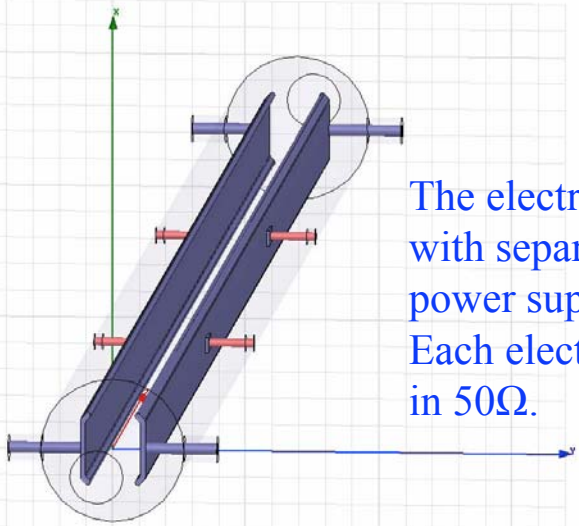
Combiner Ring Extraction Kicker

Installed CR Extraction kicker (requested for April 2006):

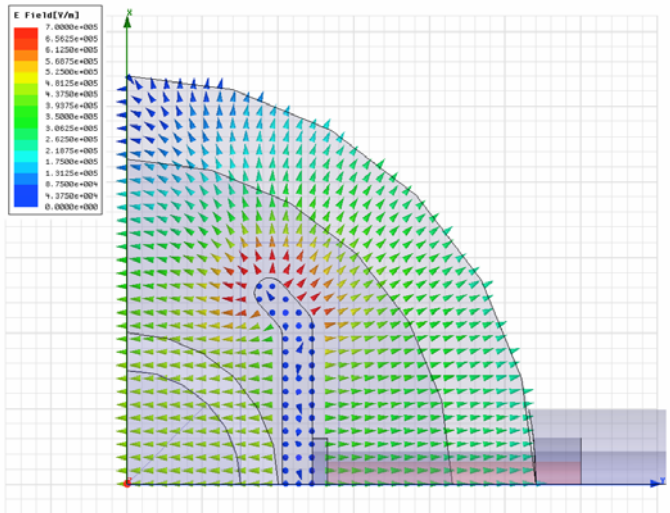
- For operation in **2006** an **existing** ex-Electron-Positron Accumulator **kicker system**, which only partially satisfies the specifications, has been modified and installed.
  - Employs 2 ferrite-cored kicker magnets whose vertical aperture is 35mm, smaller than the nominal 40mm required. The vertical restriction excluded the possibility of inserting metallized ceramic plates to improve the beam impedance.
  - Existing HV pulsed power supplies are used – using thyratron switched PFN.
  - Pulse top flatness and reproducibility remain to be measured and are not guaranteed to fulfill specifications.

Combiner Ring Extraction Kicker

- The impedance of the kicker structure seen by the beam must be such that any induced instabilities are inconsequential. The **strip-lines** of a **kicker** have been designed by CIEMAT; a paper describing the design of the strip-lines was presented at EPAC 06 [6]:



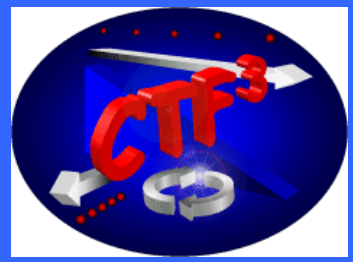
The electrodes will be pulsed with separate, opposing polarity, power supplies.
Each electrode will be terminated in 50Ω.



HFSS 3D Model of strip-lines with rectangular aperture & Predicted "E" field at middle plane

- Strip-lines should be delivered to CERN mid 2007: with installation at the earliest subsequent opportunity.
- Strip-lines could initially be pulsed with existing EPA thyratron switch.

Pulsed Power Supply for CLIC

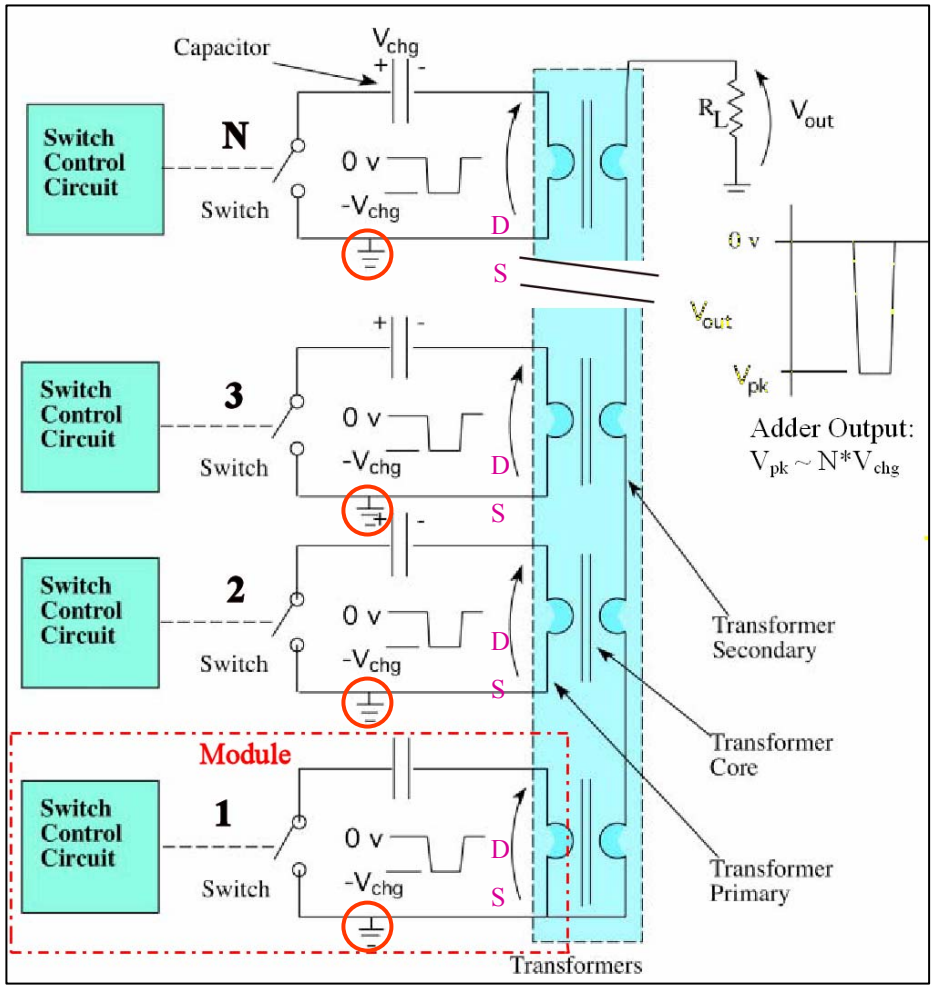


Summary of pulsed power supply requirements for CLIC:

- **Rectangular pulses, ~10 kV, up to a repetition rate of 10 MHz in burst-mode operation;**
- **To achieve required rise and fall times (≤70 ns), a solid-state switch capable of both closing and opening is required;**
- **Most fast solid-state devices that have an opening capability are relatively low voltage, e.g. MOSFETs with a rating of up to 1200 V & 22 A continuous (88A pulsed) are available (~20 ns switching time: APT 12057B2FLL_LFLL).**
- **Special circuits are required to take advantage of these fast solid-state switches, e.g.:**
  - **Inductive Adder;**
  - **Solid-state switches connected in series.**

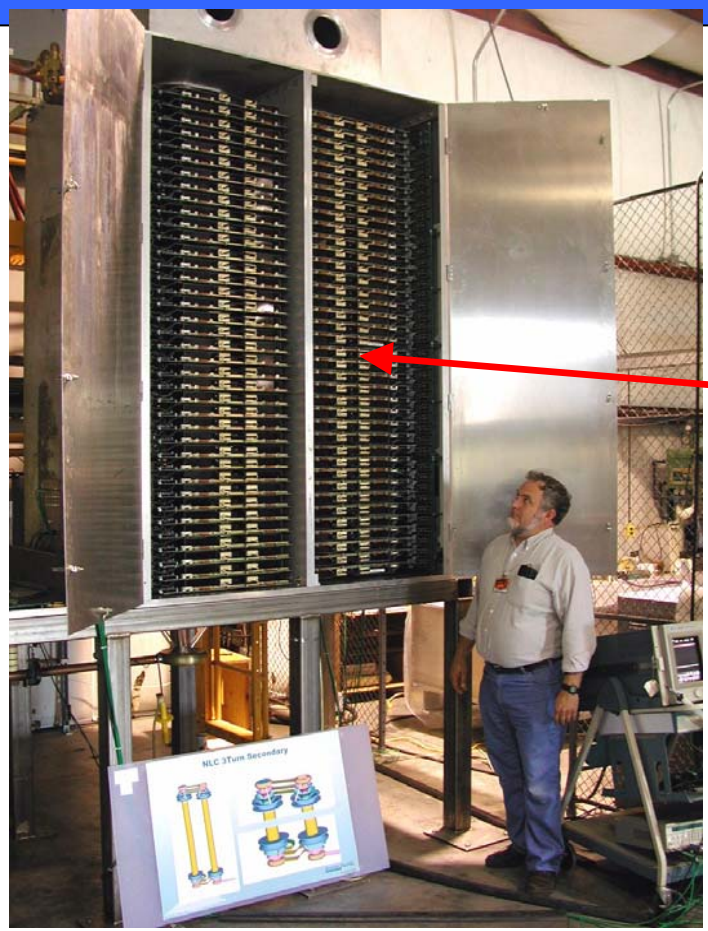
Inductive Adder

Inductive Adder, as shown below, has been developed extensively by teams lead by Ed Cook (LLNL, USA) and Dick Cassel (SLAC, USA).

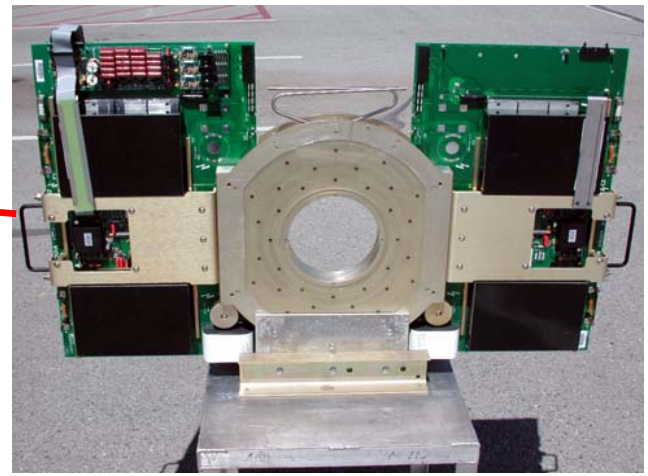


- The basic circuit used to drive the transformer primary winding consists of a capacitor and a switch. The switch is connected between the capacitor and ground.
- The switch is gated on to initiate the pulse and gated off to terminate the pulse.
- To achieve fast rise and fall times, the transformer must have very little leakage inductance: a requirement usually met by using a single turn primary winding and a single turn secondary.
- Each module provides secondary current and magnetizing current.
- The output voltage on the secondary winding is approx. the sum of the voltages appearing on each of the primary windings.

Klystron Modulator at SLAC (76 IGBT modules) – based on Inductive Adder

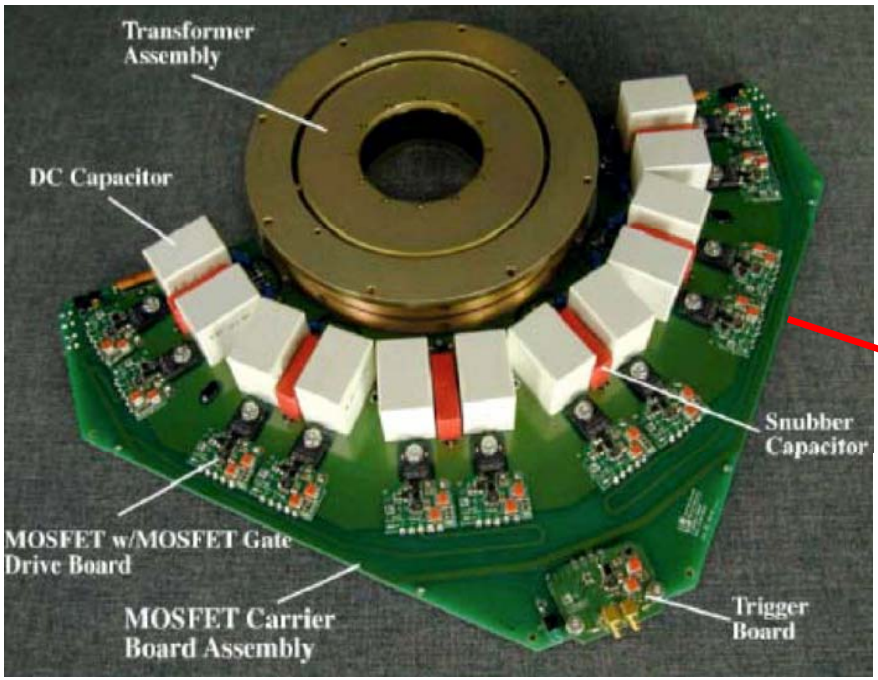


Solid-State Modulator: 3 turn secondary (Output: 500kV, 2kA, 3μs width)

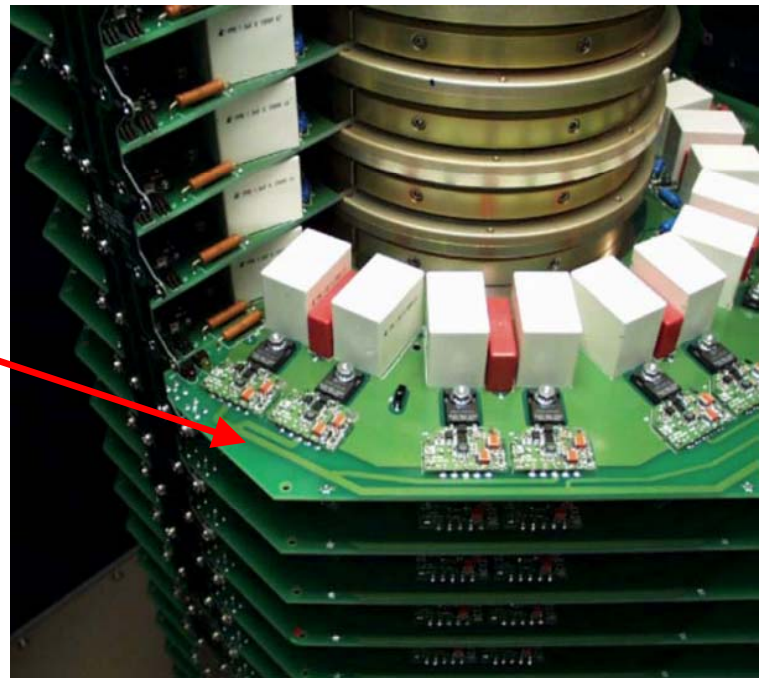


1 of 76 modules: 2 IGBTs per module

MOSFET Inductive Adder (SLAC)



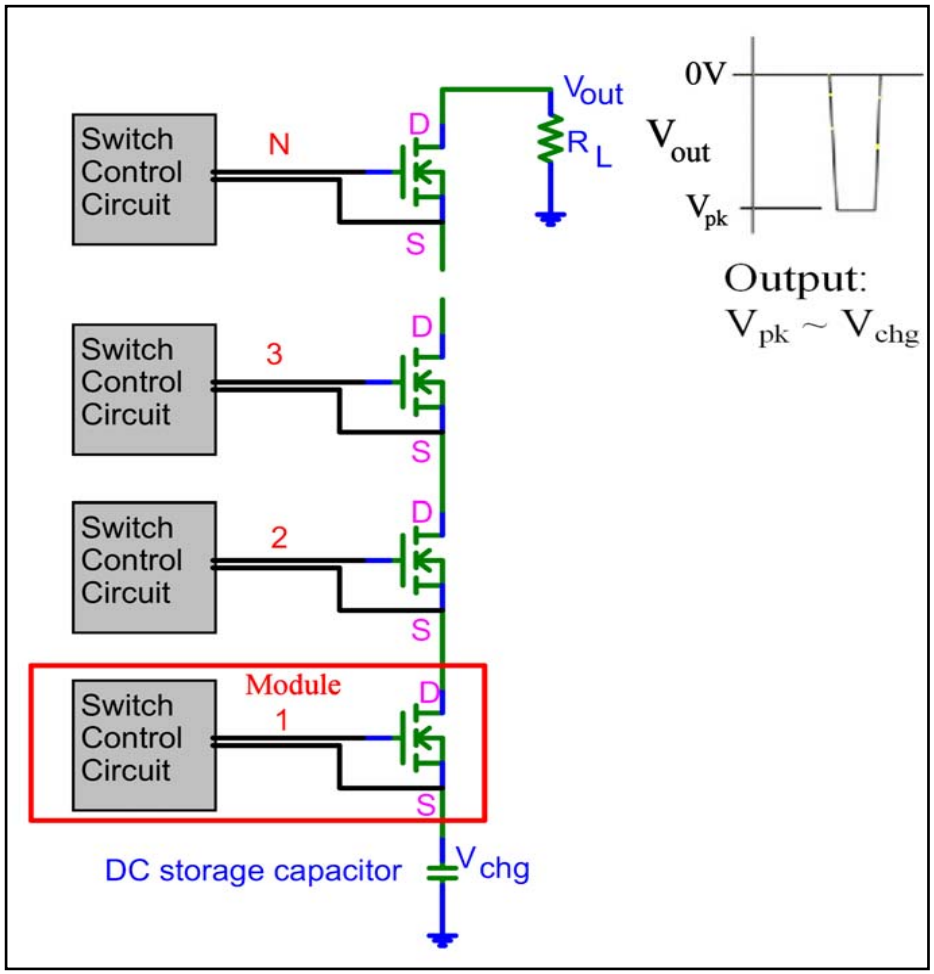
Drive Board/Transformer Module



An Inductive Adder Subassembly

Solid-State Switches Connected in Series

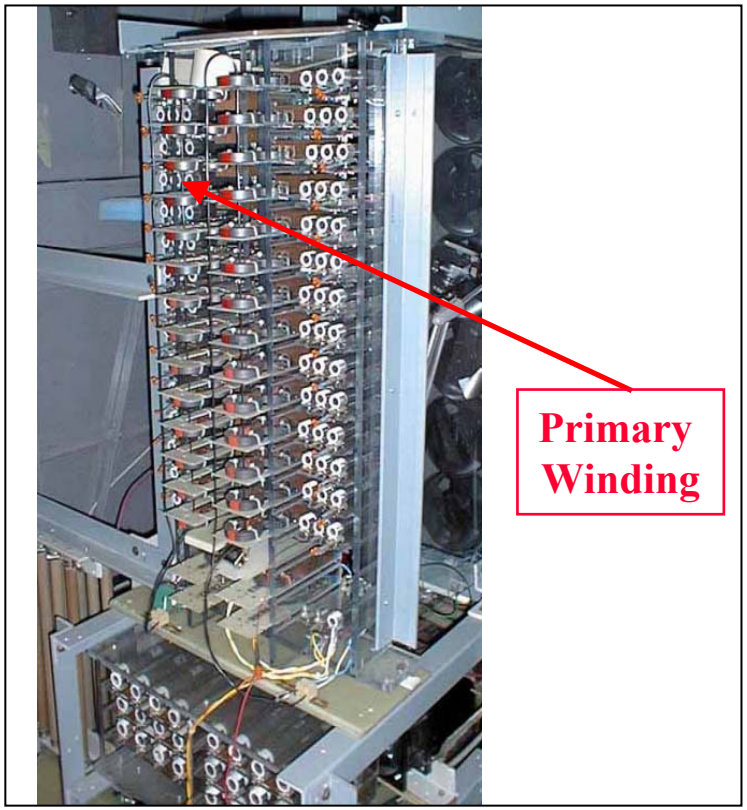
Solid-state switches consisting of stacked MOSFETs, as shown below, have been developed extensively at TRIUMF by Gary Wait & Michael Barnes.



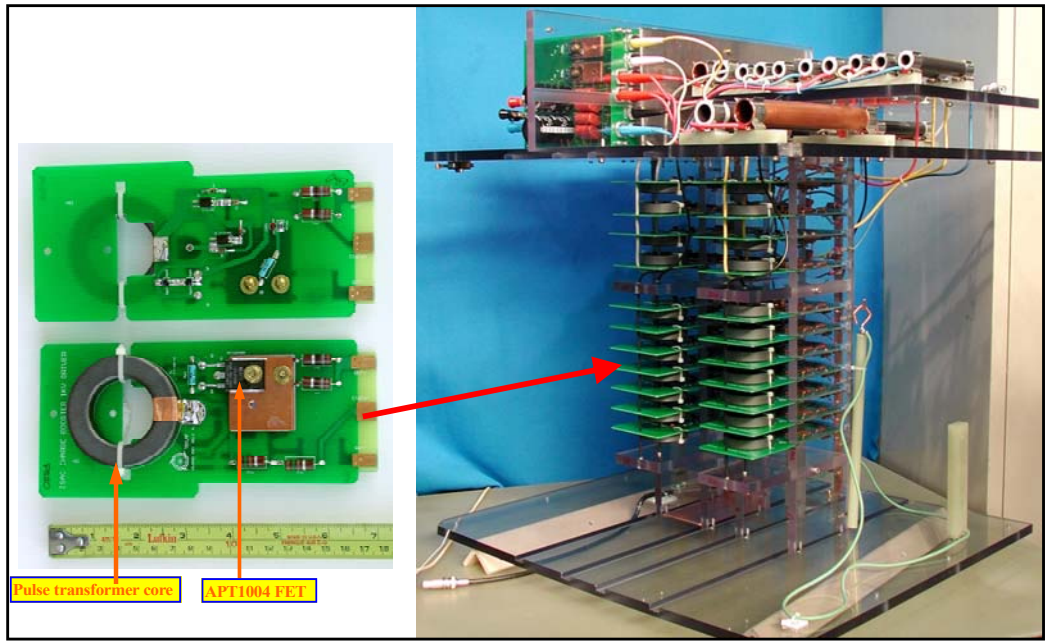
- The DC storage capacitor is charged up to the required high voltage.
- The number of series modules, including redundancy, is chosen based on the required high voltage.
- The switch is gated on to initiate the pulse and gated off to terminate the pulse.
- The switch control unit is at switch source potential, i.e. floating with respect to ground.
- To achieve fast rise and fall times, low inductance is required between the switch control unit and switch.
- Each module provides load current.
- The output voltage is approximately equal to the DC storage capacitor voltage (minus D-S voltage drops).

Example of Kickers Based on Series MOSFETs (TRIUMF)

Prototype 1MHz kicker (1995)
2 FET stacks in push-pull; *capacitive load*;
Up to 10 kV pulses; 40 ns rise & fall time;
1 MHz with storage cables (fixed rep-rate) & variable up to 0.5 MHz without storage cables.

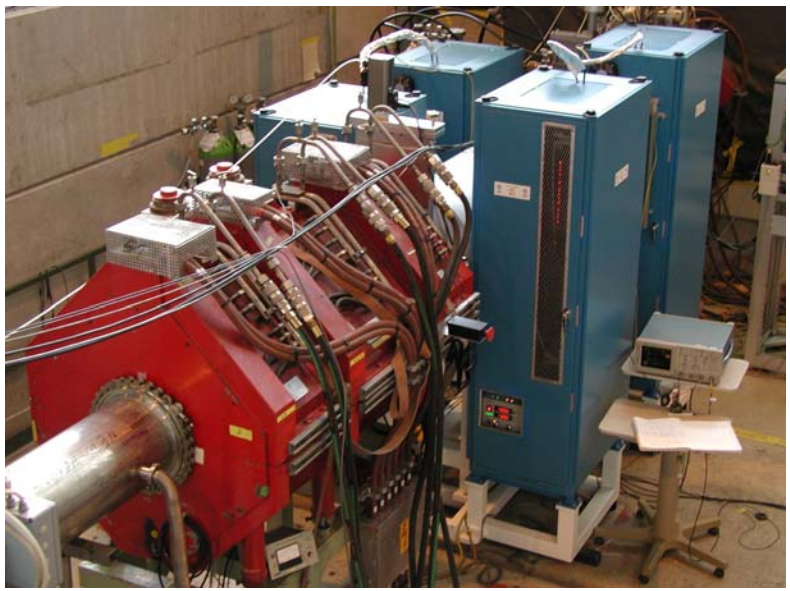


Charge Booster Kicker (2001) [(used at Grenoble (France) & TRIUMF)]
2 FET stacks in push-pull; *capacitive load*;
up to −3.5 kV; 63 ns rise & fall;
DC to 52 kHz continuous (variable);
***pulse width 350 ns to >10 s (variable)*.**

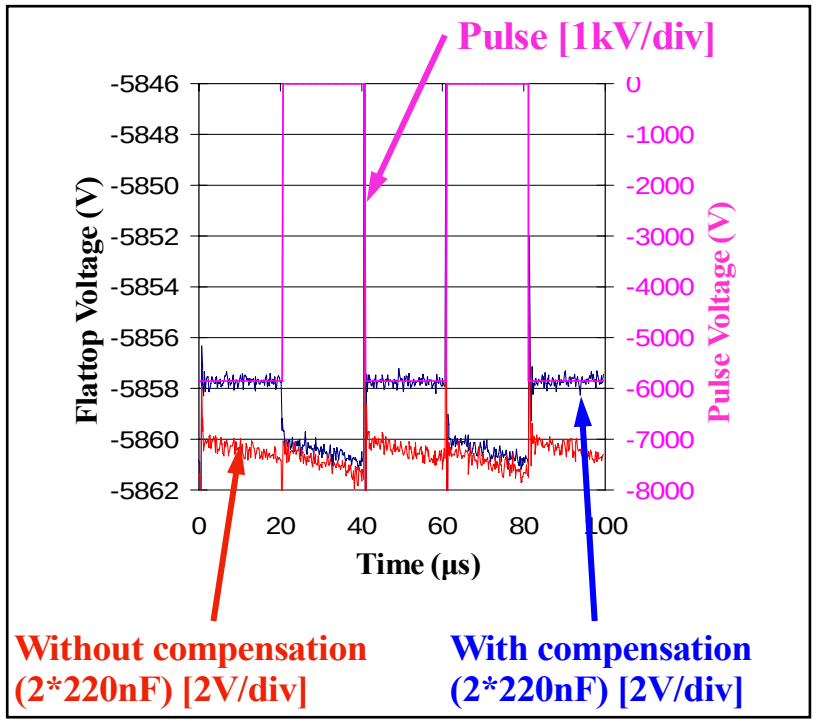


Example of Stacked MOSFET kickers continued (TRIUMF)

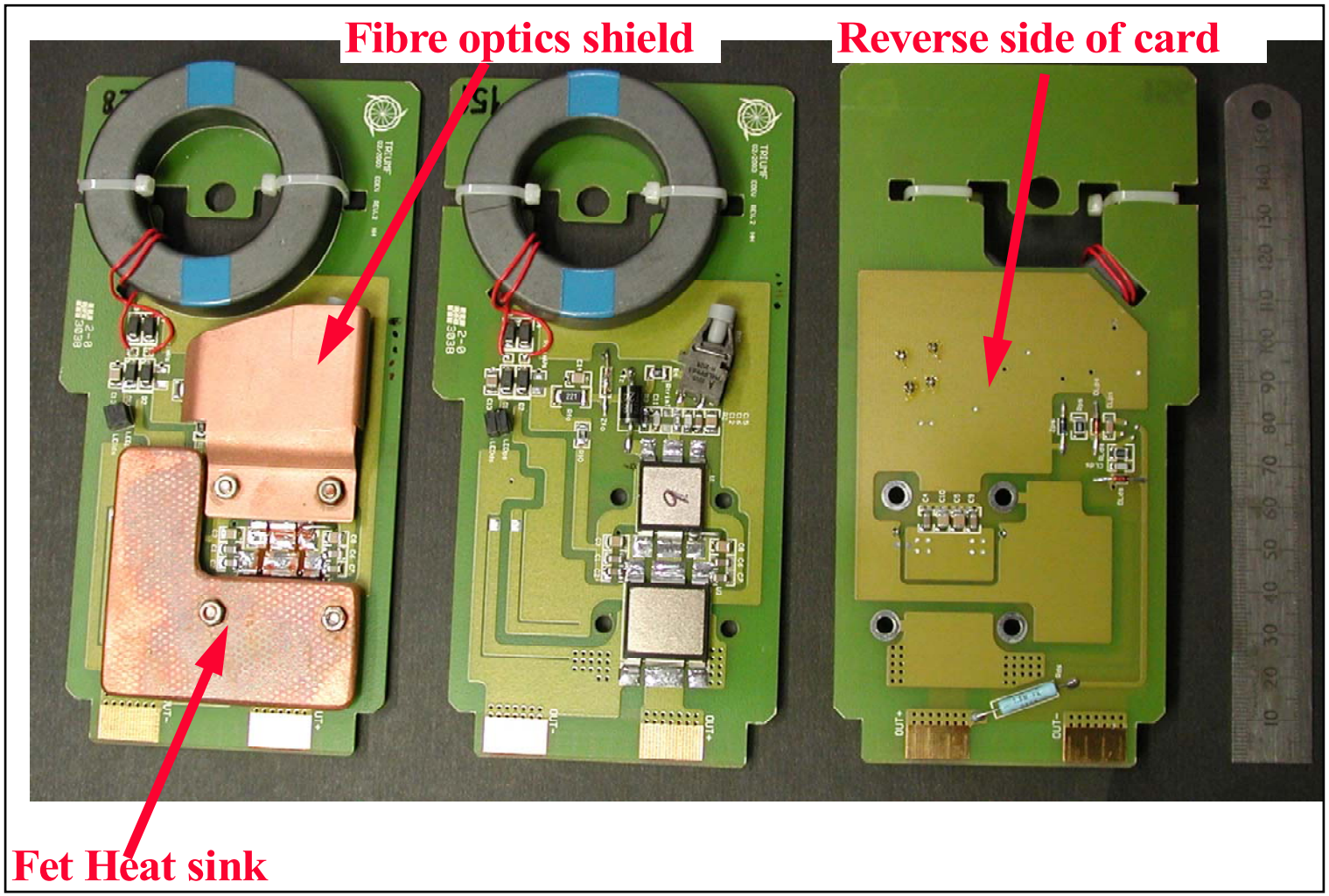
MuLan/MuCap Kicker (2003) [used at PSI (Switzerland)]
4 kicker cabinets. Each consisting of 2 FET stacks in push-pull; *capacitive load*;
±12.5 kV; 40 ns rise & fall;
DC to 77 kHz continuous;
pulse width *160 ns* to DC. Individual MOSFET cards tested to *3 MHz continuous*.



4 kickers installed at PSI for MuLan

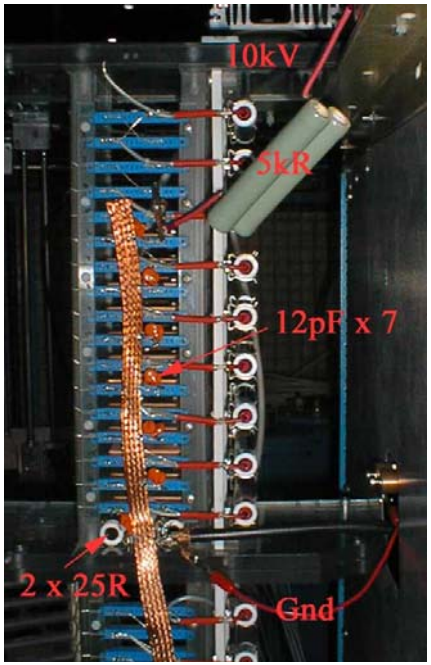


MuLan/MuCap Kicker Cards (2003)

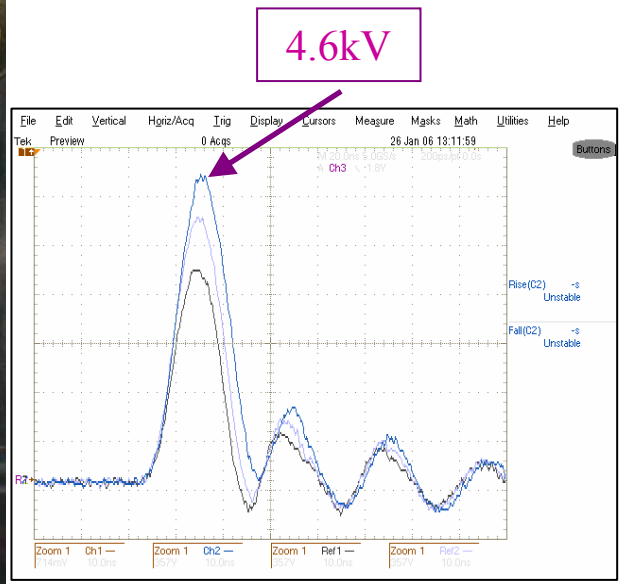


ILC Prototype Kicker (stacked MOSFETs), 2005

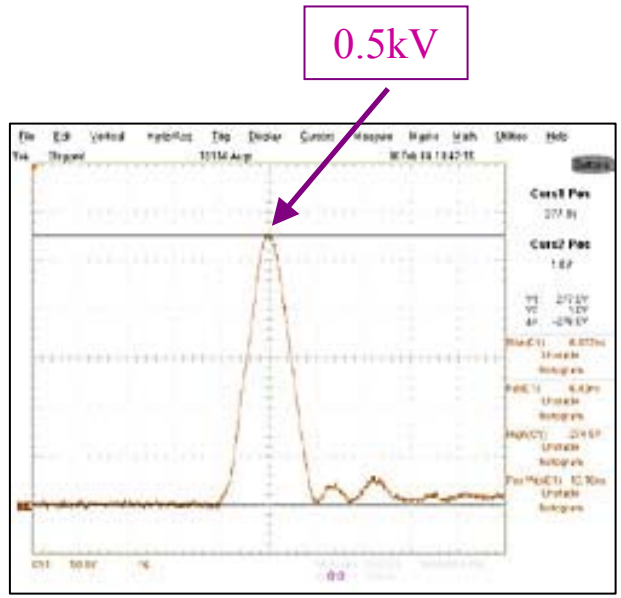
ILC prototype kicker (development at TRIUMF)
One FET stack; 5 kV pulses into a *100 Ω load*;
***6 ns rise and fall times* (10% to 90%); 1 kHz.**



One FET stack of prototype PSI kicker.

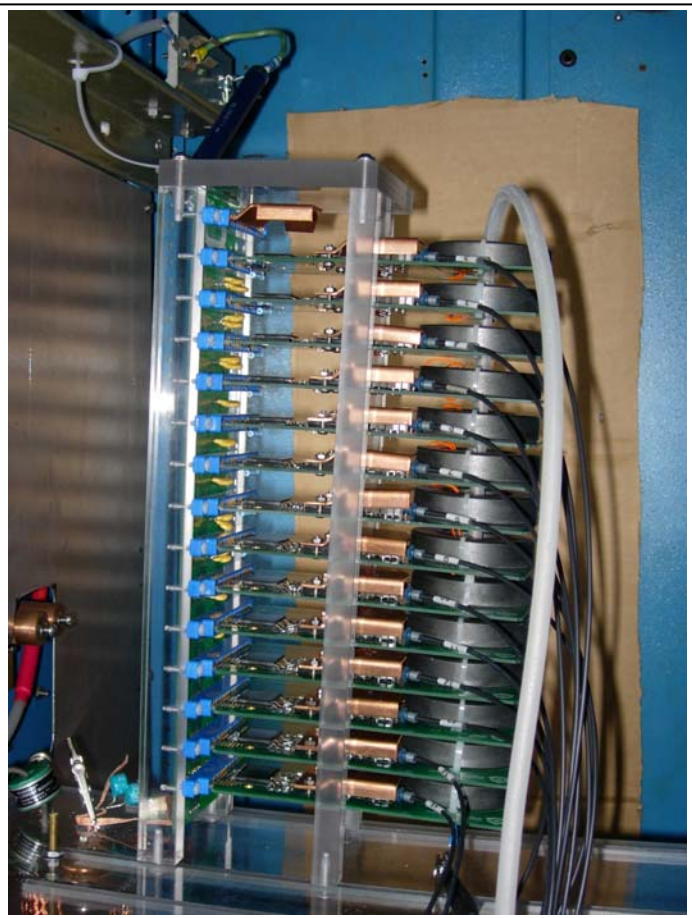


Output pulse. 10ns/div, 100 Ω load.
Post pulse noise is attributable to impedance mismatches.



Improved impedance matching (low power, low inductance, load).

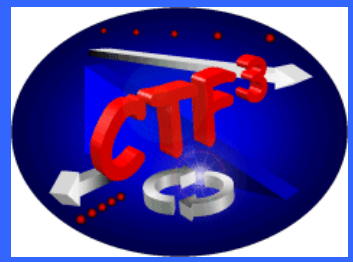
ILC Prototype Kicker (stacked MOSFETs), 2006



One FET stack of prototype ILC kicker (Rev 1).

Backplane of prototype ILC kicker (Rev 1).

Summary of TRIUMF Kickers: Stacked MOSFETs (1994-2006)

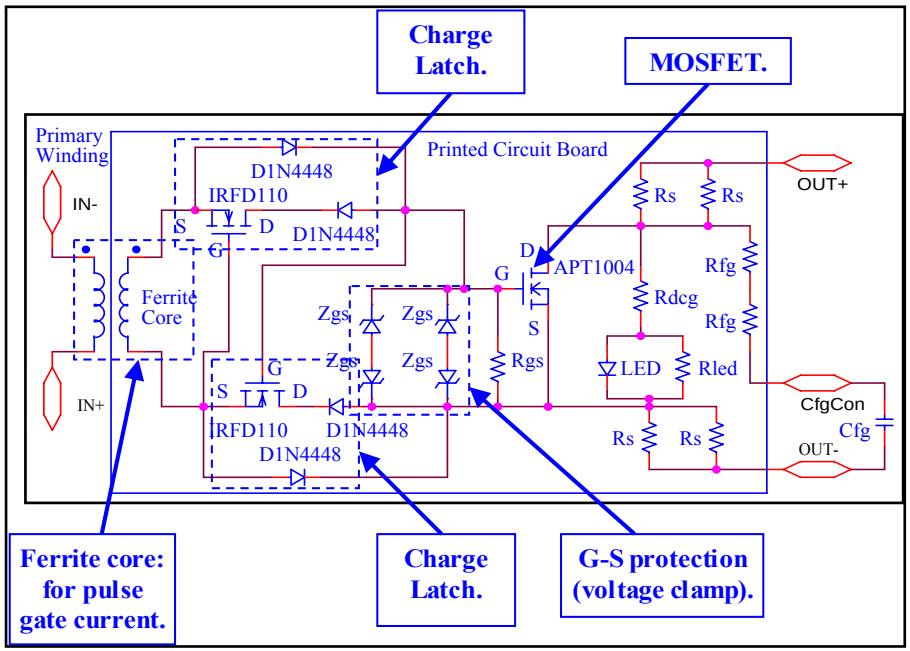


Date Built	Output Pulse Voltage	Rise & fall time (10%-90%)	Pulse Width Range	Frequency Range (continuous)	Project
1994[1]	5 kV	30 ns	250 ns to 1 s	1 Hz to 20 kHz	ISIS
1995[1]	10 kV	40 ns		Fixed: 1 MHz **Variable to 0.5 MHz**	KAON chopper
2000[1]	±10 kV	100 μs	20 ms to DC	DC to 10 Hz	ISAC Mass Sep
2001[1]	−3.5 kV	63 ns	350 ns to DC	DC to 52 kHz	Charge Booster
2003[2]	±12.5 kV	40 ns	160 ns to DC	DC to 77 kHz	MuLan/MuCap
2004[2]	0.5 kV 0.6 kV	125 ns 125 ns	50% duty 50% duty	3 MHz 2.2 MHz	TITAN RFQ
2005/6[2]	4.6 kV	6 ns		1 kHz	ILC

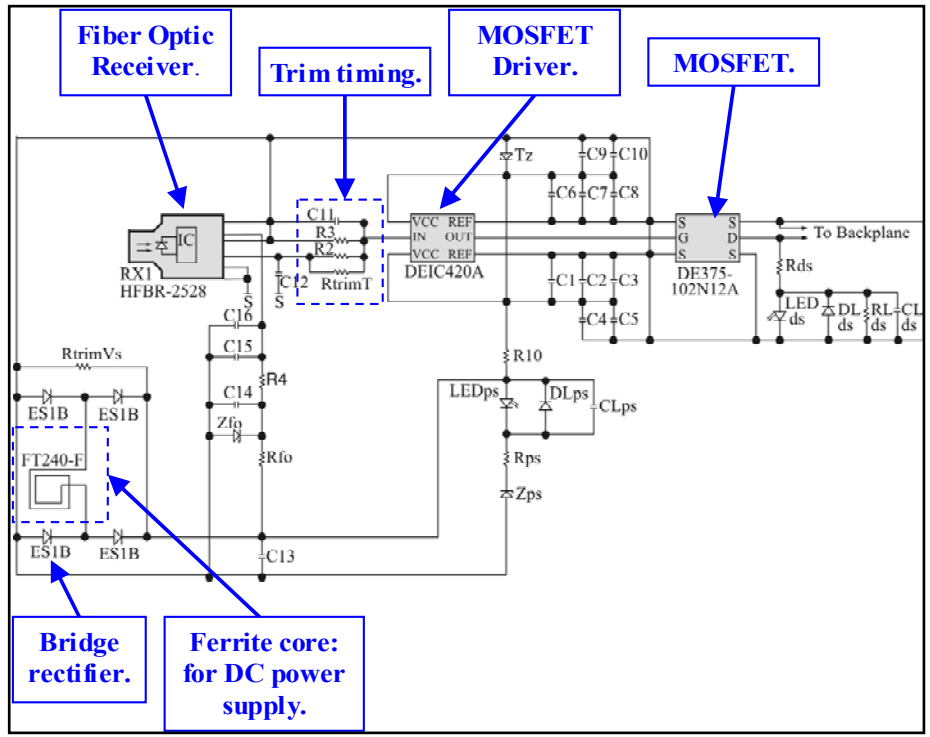
[1]: Magnetically Triggered;

[2]: Optically Triggered.

Comparison of "Old" & "New" TRIUMF MOSFET Cards

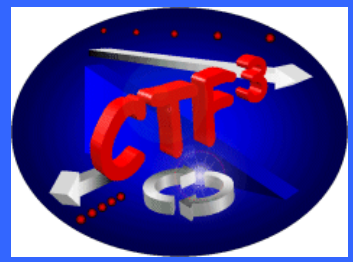


Schematic of "Old" (magnetically triggered) MOSFET Card,
with ferrite core for trigger.



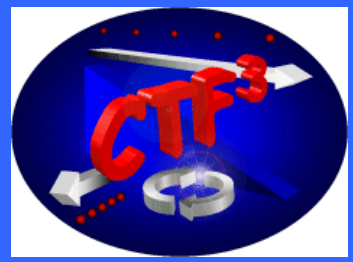
Schematic of "New" (magnetically triggered) MOSFET Card,
with fiber optic receiver & MOSFET Driver

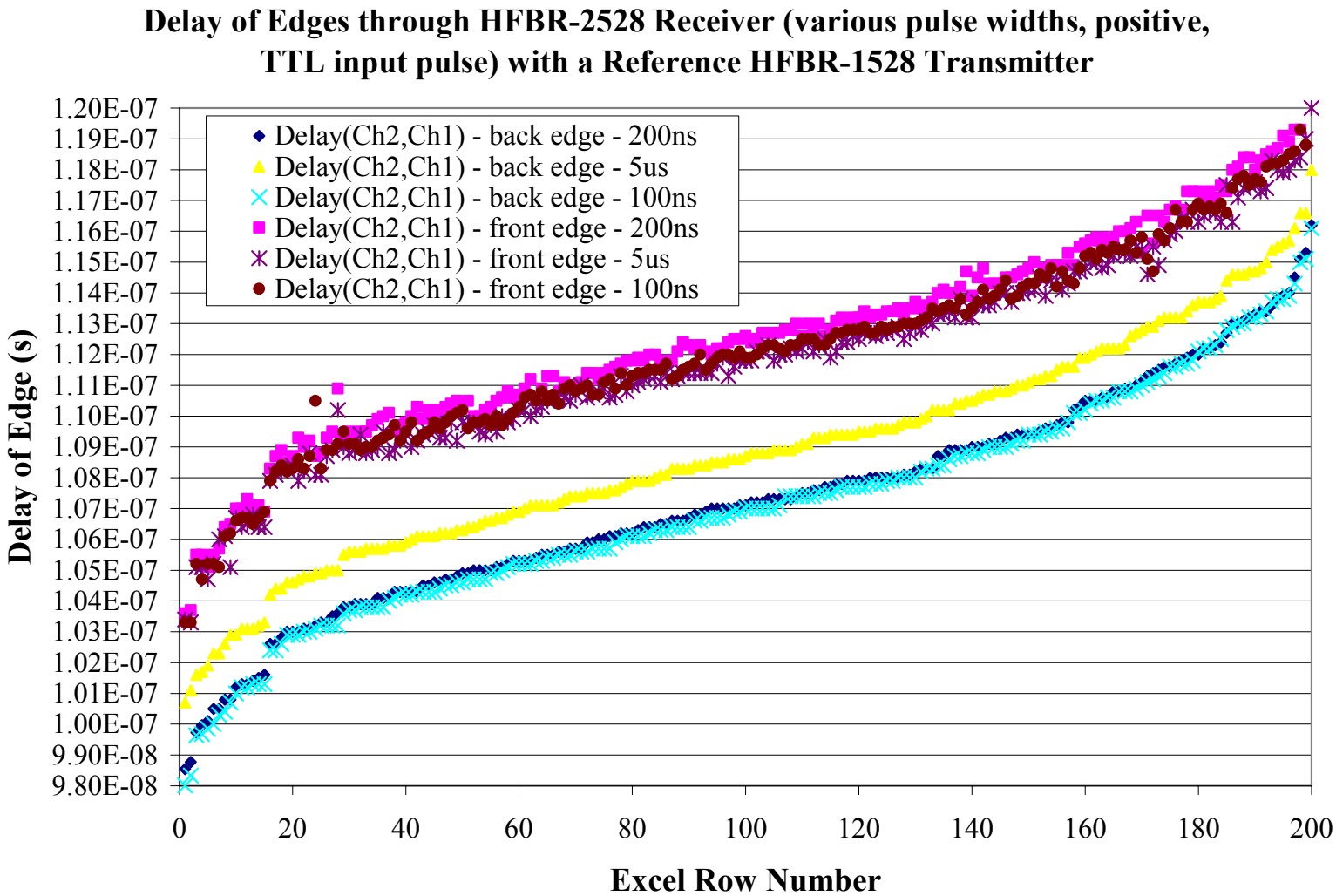
Summary re Stacked MOSFETs versus Inductive Adder[1]



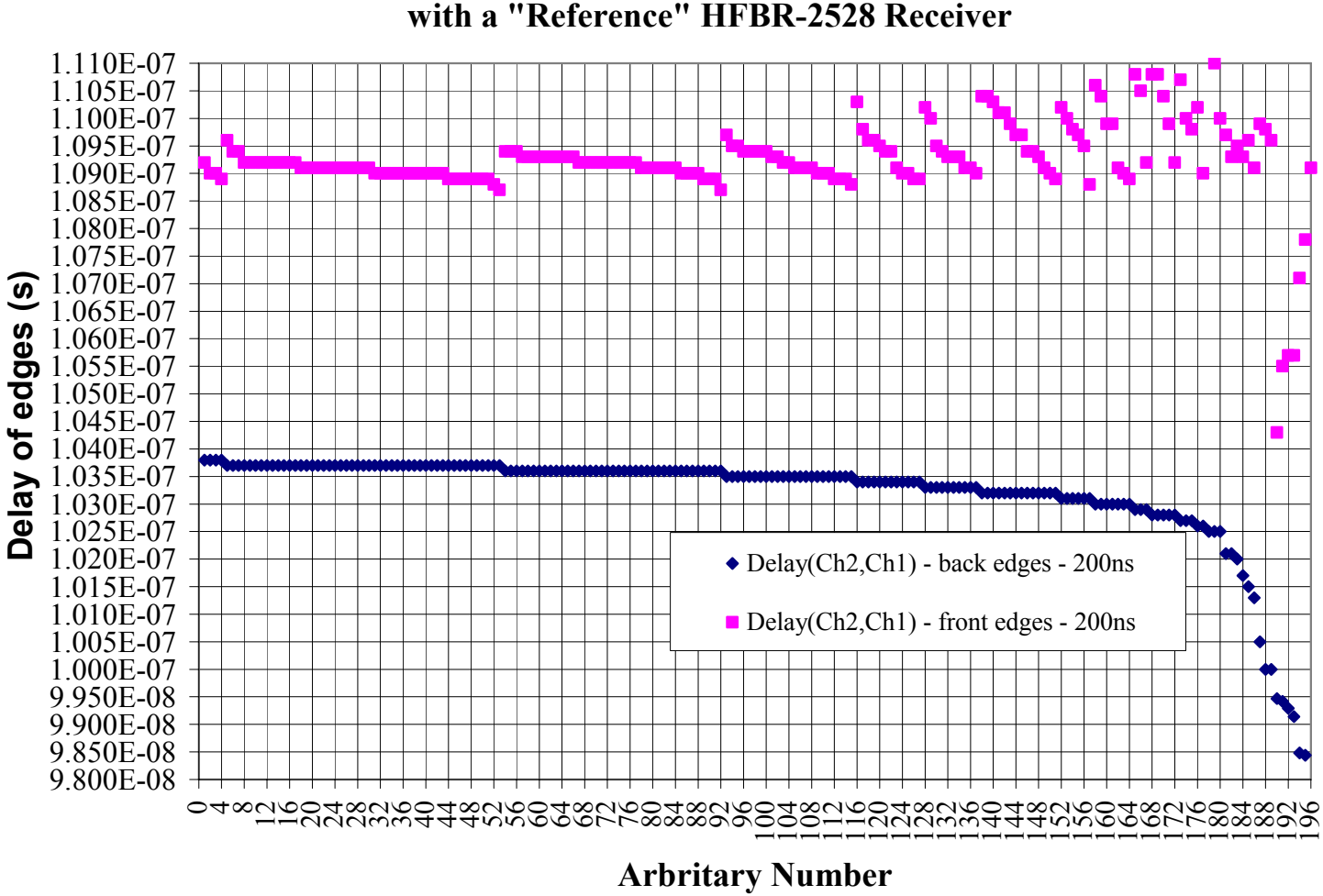
- **Stacked MOSFET circuit has advantage of no output transformer:**
  - **No contribution, from this source, to pulse flat-top DROOP (specification <±0.25%);**
  - **No transformer reset required;**
  - **No contribution, from transformer saturation, to fault current magnitude.**
- **Inductive adder circuit has advantage of gate circuit being referenced to ground:**
  - **Relative timing of MOSFET switching is considerably easier;**
  - **Fast-grading may (or may not) be required for stacked MOSFETs.**
- **Advantages and disadvantages of both methods:**
  - **No clear "winner";**
  - **Further work required to identify best candidate;**
  - **A work-package, to examine the main disadvantage of the series connected MOSFET topology, is in the final stages of negotiation.**

HFBR-2528 Fiber Optic Receiver Delay

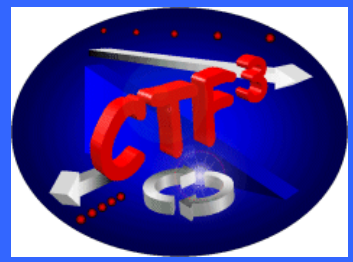




HFBR-1528 Fiber Optic Transmitter Delay

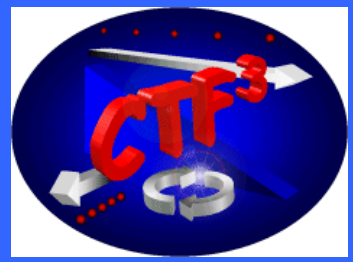


Present Trigger Technique for "New" MOSFET card.



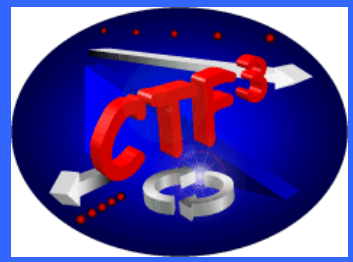
- For the MuLan/MuCap kicker design, which uses the HFBR-2528 fiber optic receivers, the strip-lines were open-circuit (i.e. a capacitive load);
- Hence the timing of only the turn-on command edge was important and this could be set-up using an RC network;
- However, for CTF3 & CLIC (current to be turned on and off), the workability of stacked MOSFETs depends upon minimal pulse width distortion (this is not the case with the HFBR-2528 fiber optic receivers presently used).

Work Package #1: Objectives



- **Initial efforts of work package #1 focus on the Stacked MOSFET topology. The optically triggered TRIUMF MOSFET card, with a MOSFET driver on each card, presently seems a better approach than the magnetically triggered circuit.**
- **Improved triggering techniques are required to satisfy the stringent timing constraints for both turning-on and turning-off the power MOSFETs for both CTF3 & CLIC strip-line kickers; this is the main goal of work package #1, dated July 2006.**

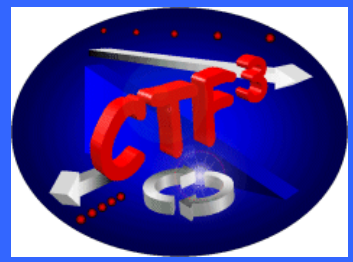
Work Package #1: Development of Trigger Techniques



Options for triggering the MOSFETs, so as to minimize pulse width distortion (PWD), that warrant further investigation, are:

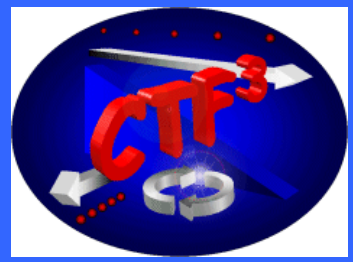
- **More appropriate fiber optics than the HFBR-1528 & HFBR-2528 (PWD 5 ns to 15 ns measured);**
- **Using a second ferrite, that is independent of the power supply ferrite, to magnetically couple the trigger signal;**
- **Magnetically couple the trigger signal through the power supply ferrite and use a "masking circuit" to discriminate the trigger pulse from the charging current.**

Conclusions

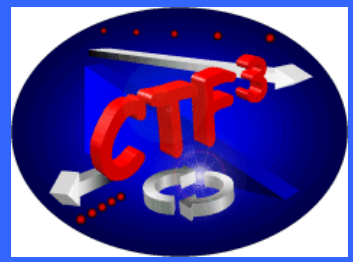


- A temporary kicker system (ex e+ and e- injection into EPA) is presently installed for the CTF3 CR extraction kicker.
- CIEMAT have designed the strip-line electrodes for a new CTF3 CR extraction kicker: strip-lines to be delivered to CERN mid 2007, with installation at the earliest subsequent opportunity.
- Two solid-state approaches for the CTF3 CR extraction kicker and CLIC kicker have been examined:
  - MOSFET inductive adder (SLAC/LLNL);
  - Series connected MOSFETs (TRIUMF).
- Both approaches have advantages and disadvantages.
- Means of satisfying the **stringent timing constraints,** of the series connected MOSFETs approach, are being examined; this is the goal of work-package #1, which is in the final stages of negotiation.

Questions ??

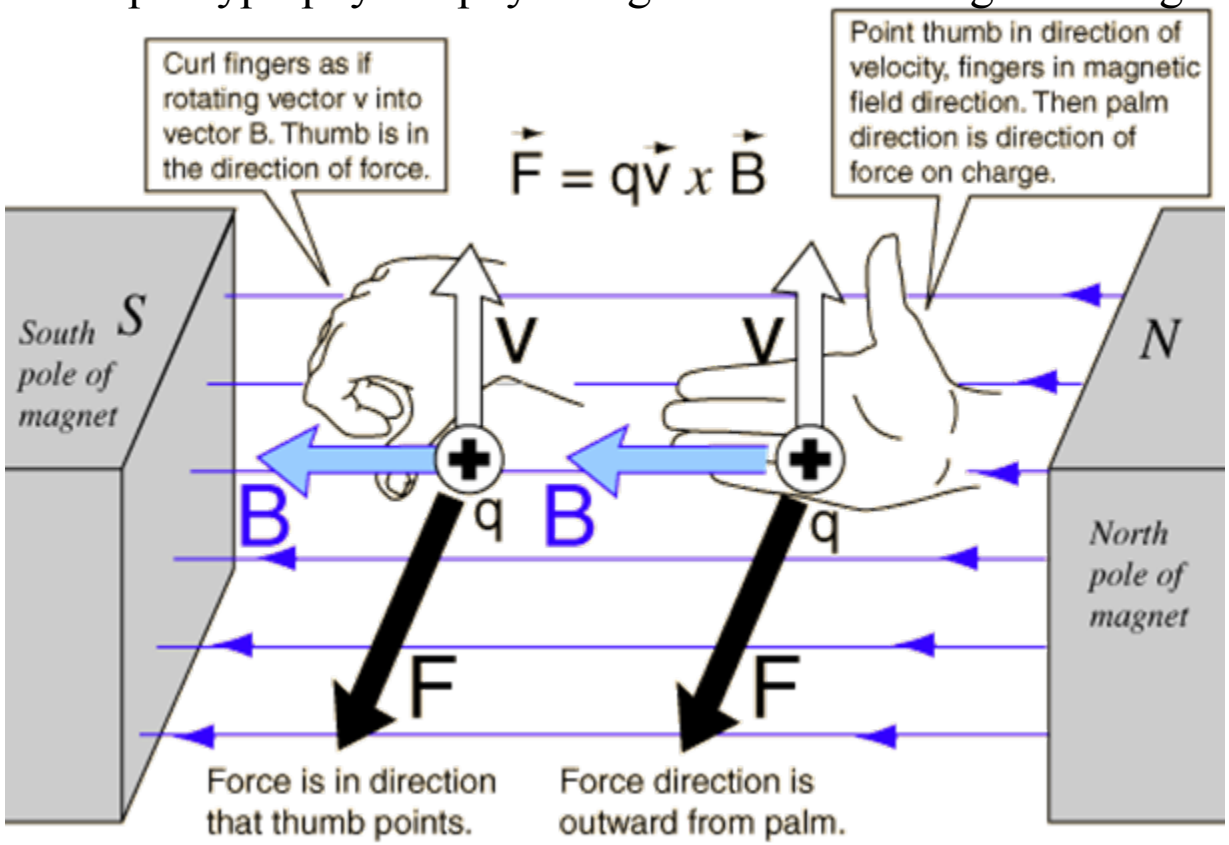


Magnetic Force as given by Lorentz Force Law



Right Hand Rule (for moving positive charge)

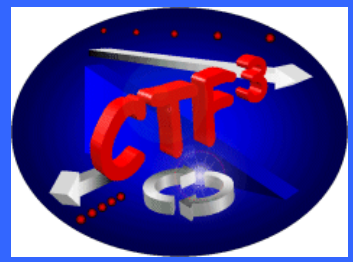
Ref: http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/magfor.html



References

1) M.J. Barnes, “CTF3 Strip-line Kicker”, slightly modified version of presentation made at CIEMAT, file date May 10 2006, https://edms.cern.ch/document/734146/1
2) M. J. Barnes, G. D. Wait, “A 25 kV, 75 kHz, kicker for measurement of muon lifetime”, IEEE Transactions on Plasma Science, Vol. 32, No. 5, October 2004, pp1932-1944.
3) Agilent: www.agilent.com.
4) Directed Energy Inc. (DEI), USA, www.directedenergy.com
5) M.J. Barnes, G.D. Wait, “A FET Based mass separator kicker for TRIUMF ISAC project”, Proc. of the Seventh European Particle Accelerator Conference (EPAC 2000), 26-30, June 2000, Vienna, Austria, pp2376-2378.
6) I. Rodríguez, L. García-Tabarés, F. Toral, A. Ghigo, F. Marcellini, “Design of a Strip-Line Extraction Kicker for CTF3 Combiner Ring”, Proc. of the Tenth European Particle Accelerator Conference (EPAC 2006), June 2006, Edinburgh, Scotland.

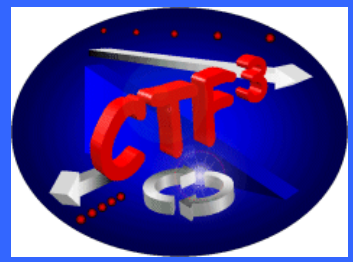
WP1: Fiber Optic System



A suitable fiber optic system must be capable of:

- **Operation over a large dynamic frequency range. The receiver should, ideally, be DC coupled;**
- **Ideally no output amplifier is necessary, hence output of receiver should satisfy (digital, not analogue ??) :**
  - **High level output voltage of 4.2 V min.;**
  - **Low level output voltage is 0.4 V max.**
- **Fast slew rate of output (to minimize switching delays associated with different threshold levels of the input of the DEIC 420);**
- **Reliable connector between fiber optic cable and transmitter/receiver;**
- **Low pulse width distortion (preferably ≤ 0.5 ns for pulse widths of <50 ns to DC).**
- **Very low temperature coefficient, i.e. minimal change in pulse width, output voltage levels, and slew rate with temperature.**

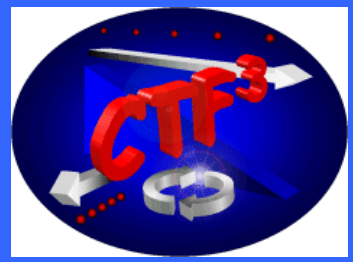
WP1: Dedicated Ferrite-Coupled Trigger



Remove the fiber optic receiver from each card and, instead, trigger the MOSFET driver via a second ferrite:

- **The second ferrite would have similar dimensions to the existing power supply ferrite (dimensions 2.4” outside diameter, 1.2” inside diameter and 0.5” high).**
- **A charge latch circuit similar to that used in previous, magnetically coupled, TRIUMF designs could be used to maintain the required high and low input voltage levels to the MOSFET driver.**
- **Voltage clamps, with high “off-state” resistance, would be required on the input to the MOSFET driver to ensure the input voltage pulse is ALWAYS in the range: −5 V to Vcc+0.3 V.**

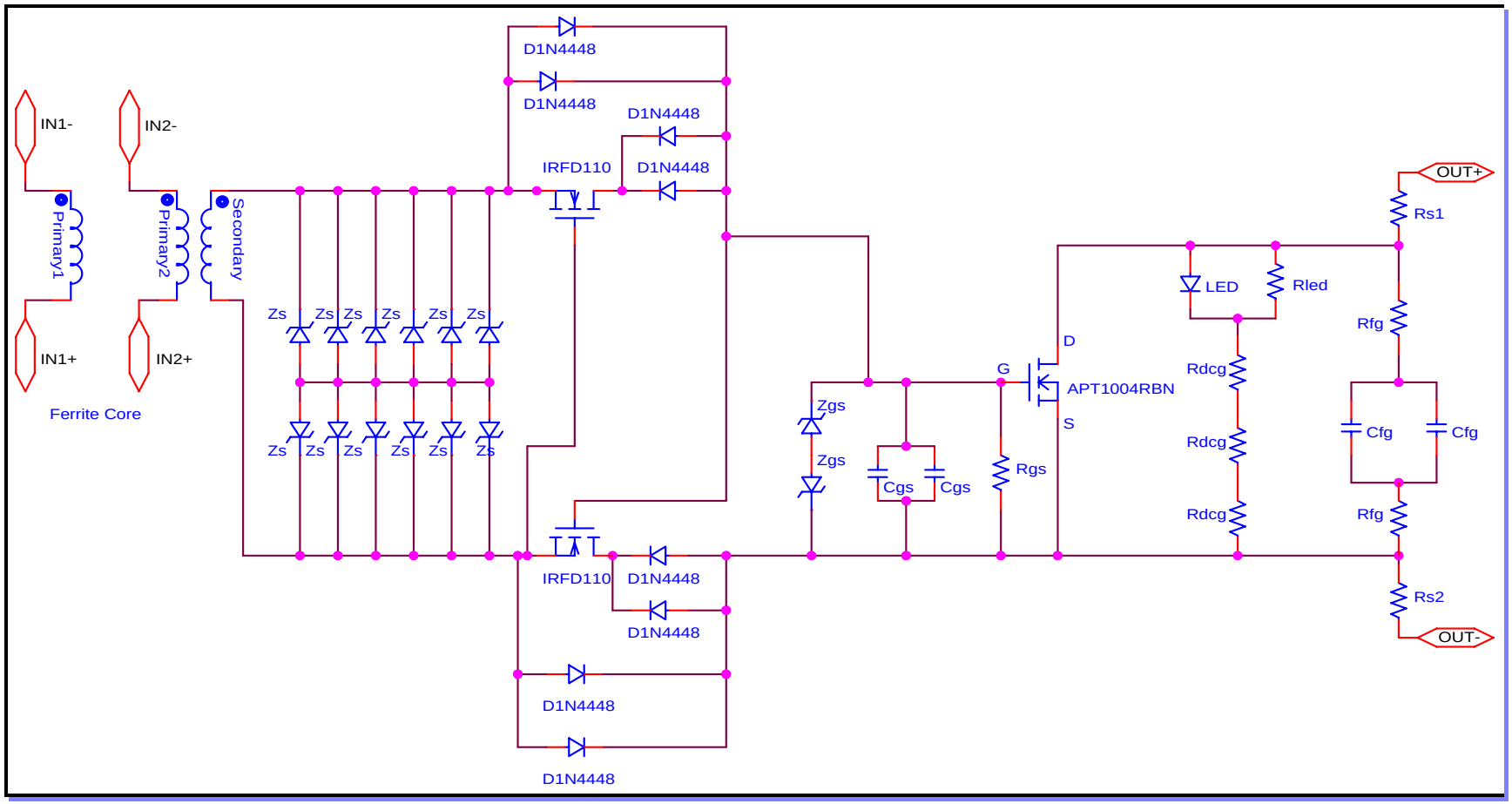
WP1: Shared ferrite-coupled trigger & LV power supply



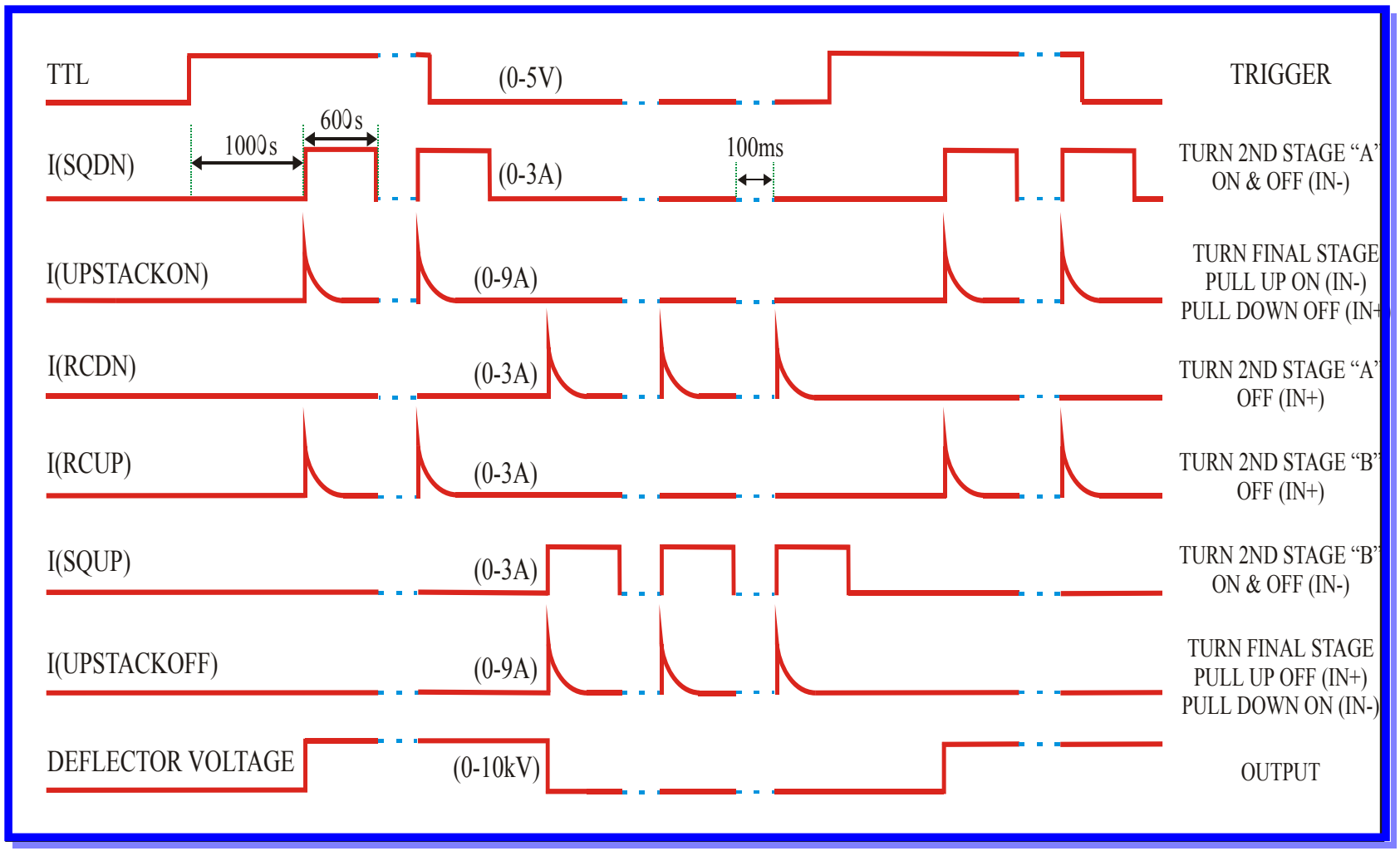
Remove the fiber optic receiver from each card and, instead, trigger the cards via the existing "power supply" ferrite:

- **The "command current pulse" will also provide energy to the on-card DC power supply;**
- **The "command current pulse" will have a fast leading edge and an RC decay for the falling edge, i.e. as per [5];**
- **The leading edge of the command current pulse will transfer power to the on-board DC power supply;**
- **A fast rising edge of the command current pulse will act as an "on-trigger" to the MOSFET driver;**
- **A fast falling edge of the command current pulse will act as an "off-trigger" to the MOSFET driver;**
- **The RC decay time will be chosen to be slow enough so as not to appreciably change the magnitude of input voltage to the MOSFET driver. Hence this RC decay does not change the state of the MOSFET driver [5];**
- **A charge latch circuit similar to that used in previous, magnetically coupled, TRIUMF designs could be used to maintain the required high and low input voltage levels to the MOSFET driver.**
- **Voltage clamps, with high "off-state" resistance, would be required on the input to the MOSFET driver to ensure the input voltage pulse is ALWAYS in the range: −5 V to Vcc+0.3 V.**

Magnetically Coupled Final Stage for MOSFET Kicker

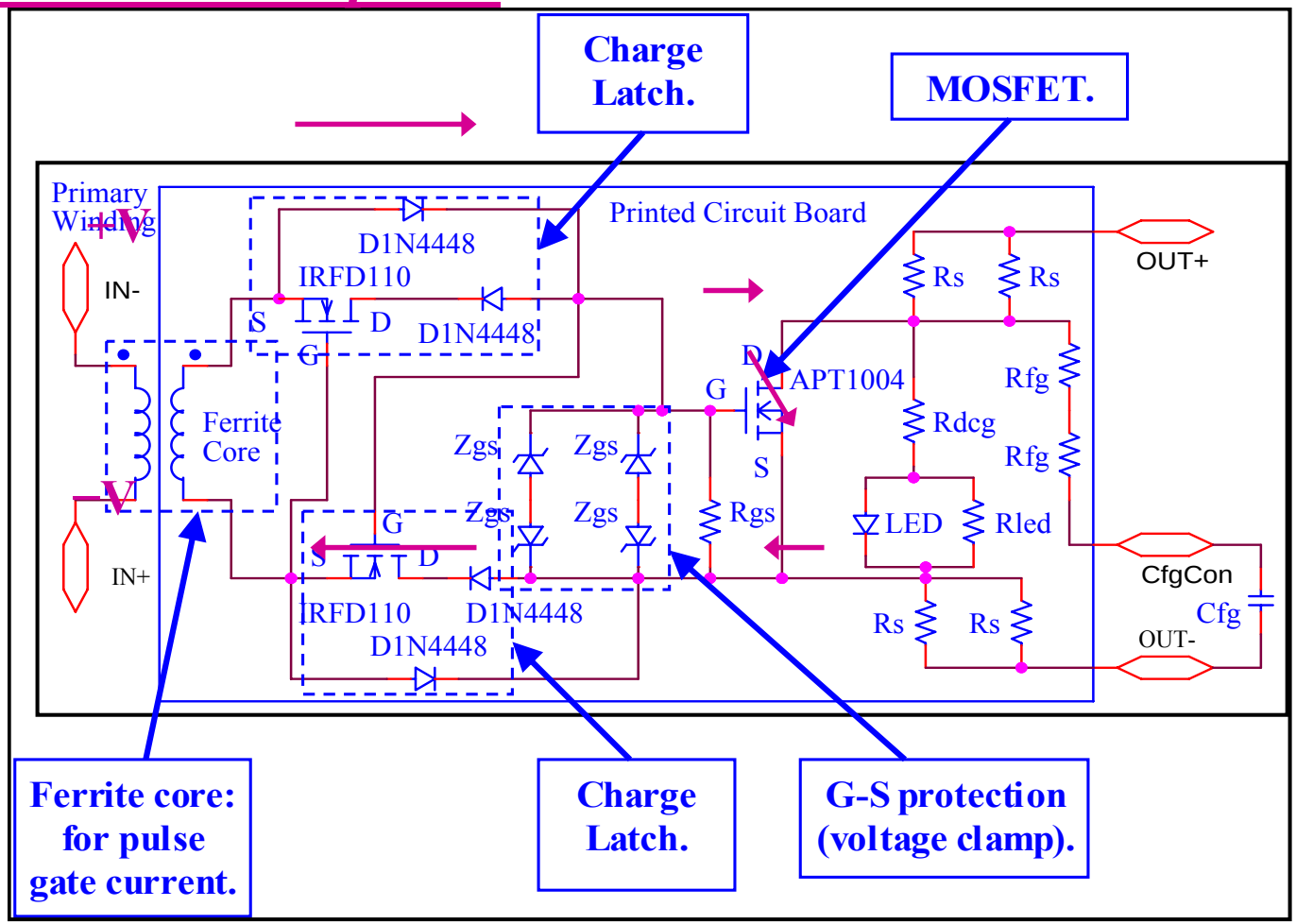


Example pulse patterns for MOSFET Based Kicker



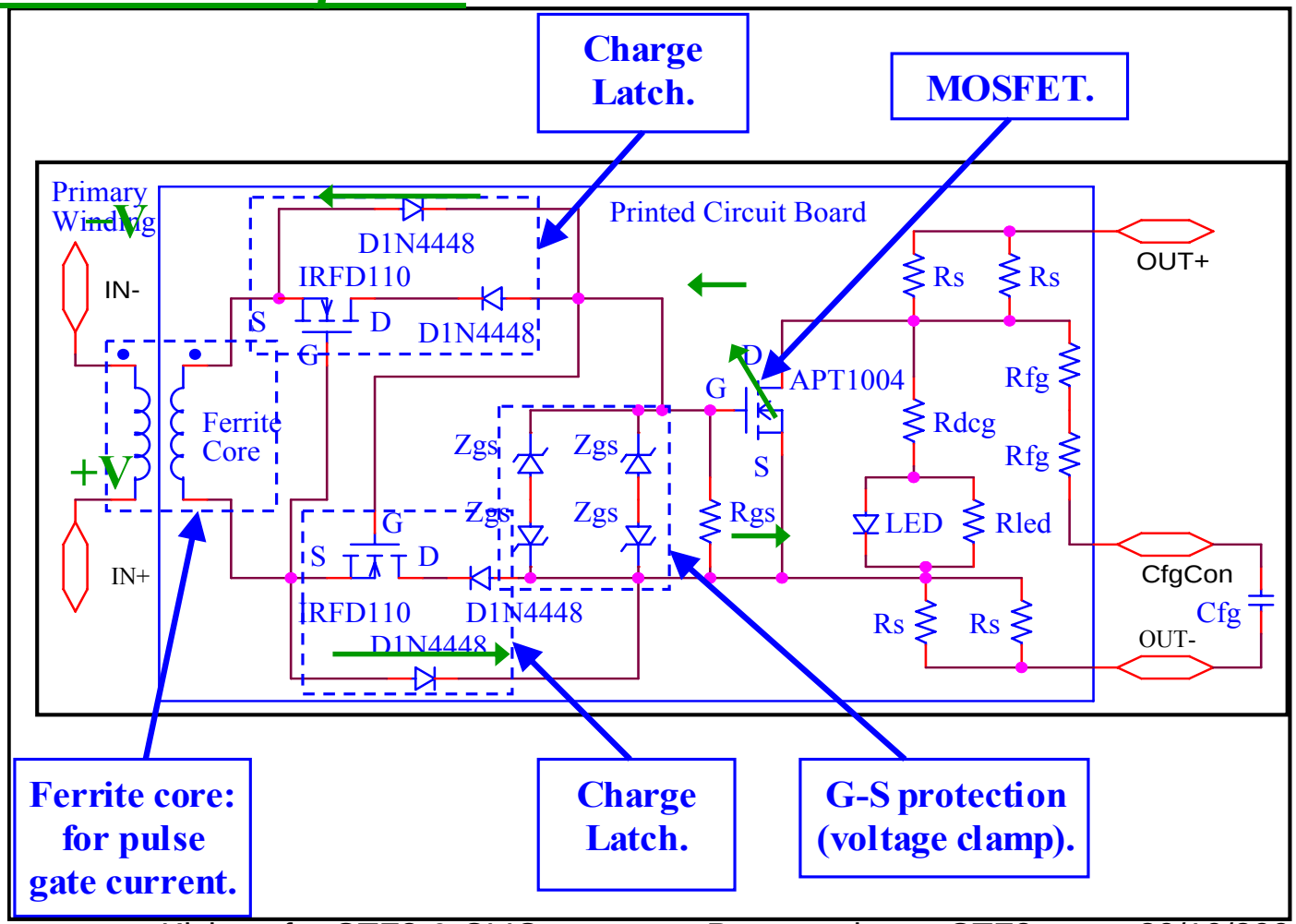
Schematic of "old" TRIUMF MOSFET card

Turn-on command *pulse*:

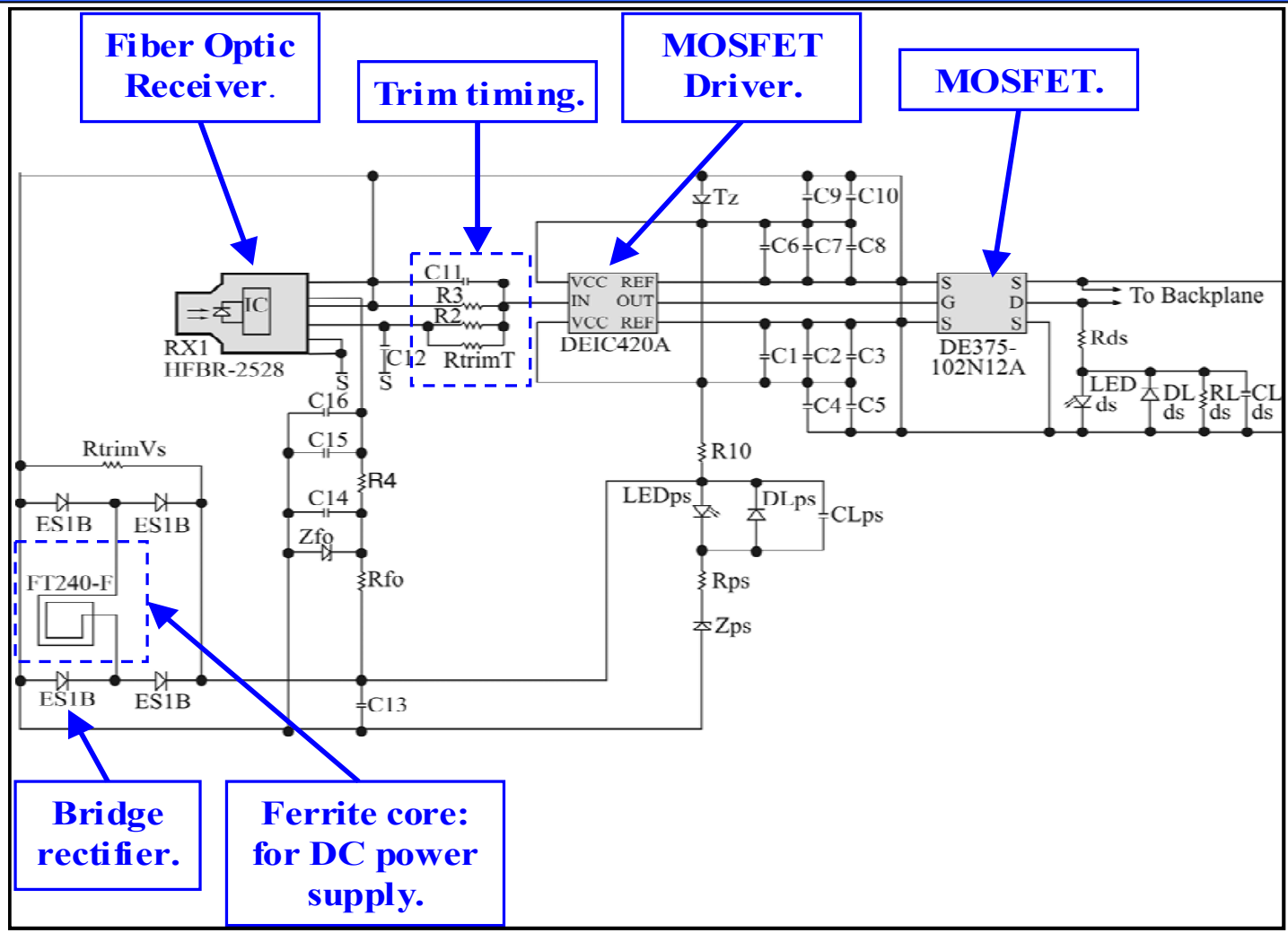


Schematic of "old" TRIUMF MOSFET card

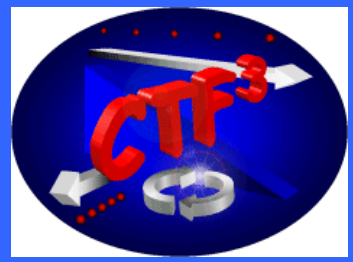
Turn-off command *pulse*:



Schematic of "new" TRIUMF MOSFET card



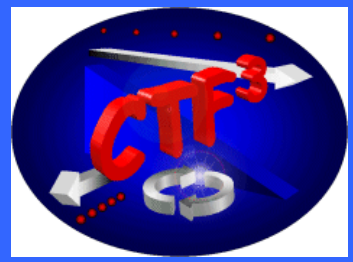
Comparison of "Old" & "New" TRIUMF MOSFET Cards



Ideally: high current, low inductance, source to rapidly switch MOSFET (to supply, in particular, Miller Charge). Hence "new" card is best candidate; however …….

	Old Style (Gating via pulse transformer)	**New Style (Fiber Optics)**
Gate Drive Current	Used to supply up to approximately 3 A.	MOSFET driver capable of supplying 20A peak
Pulse transformer required for pulse gate-source current	Yes	Indirectly: via DC supply and MOSFET driver
Parasitic inductance	Leakage inductance of ferrite and parasitic inductance of primary circuit dominate.	Very low parasitic inductance between output of MOSFET driver and gate-source. Leakage inductance of ferrite relatively unimportant.
Gate drive circuit output resistance	Preferably high so as to act as a current source.	Typically: 0.4 Ω Maximum: 0.6 Ω
Voltage clamp required gate-source	Yes	No
Experience	Reliable	Can collapse 1000 V in 3 ns (slowed down to reduce RF noise and limit dV/dt across off-state cards)
Primary winding	Care taken to minimize propagation delay through primary winding so as to minimize differences in timing of turn-on command. Current transients, during switching, superimposed on primary "command" pulse modify switching.	Propagation delay through primary winding unimportant. Current transients, during switching, superimposed on primary "command" pulse but relatively unimportant.
Fiber optics	No	Yes: spread in delays MUST be compensated for. **Pulse width distortion will be a problem too. More appropriate fiber optics available??**

Comparison of MOSFETs



MOSFET	Generation	Volts	Ipulse	Pd (W)	Package	Iar	Idss (25C) [Vds=Vdss]	Idss (125C)	Qgd (typ) [0.5Vdss]	Qg (typ)	Coss (pF)	Tjc (C/W)	Rise Time (ns)	Fall Time (ns)	Turn-on delay (ns)	Turn-off delay (ns)	Qrr (uC)	Rds(on) (Ohms)
DE150-102N02		1000	11	80								1.25	4	4	4	4		
IRFPG30		1000	12	125	TO-247	3.1	100uA	500uA	42nC	80nC		1	24	29	12	89	1.3	
IRFPG40		1000	17	150	TO-247	4.3A	100uA	500uA	65nC	120nC		0.83	33	30	15	100	1.9	
APT1004	**4**	**1000**	**17.6**	**180**	**TO-247**		**250uA**	**1mA**	**18nC**	**35nC**	**115**	**0.68**	**10**	**14**	**12**	**33**	**1.65**	
IRFPG50		1000	24	190	TO-247	6A	100uA		110nC	190nC		0.65	35	36	19	130	3.5	
IXFH6N100F (IXYS)		1000	24	180	TO-268 & TO-247	6	50uA (80% Vdss)	1mA	22nC	54nC		0.25	14	14	12	32	0.8	
APT1201R6BVR	5	1200	32	280	TO-247	8A	25uA	250uA	78nC	155nC		0.45	10	15	12	50	7	
APT1201R4BLL	7	1200	36	300	TO-247	12A	100uA	500uA	48nC	91nC	309	0.42	9	23	14	44	7	
APT1001	4	1000	44	310	TO-247		250uA	1000uA	47nC	90nC	360	0.4	16	24	15	64	4.5	
APT10090BLL	7	1000	48	300	TO-247	12A	100uA	500uA	52nC	78nC	338	0.42	5	8	10	26	9	
DE275-102N06A		1000	48	375		6A	50uA (80% Vdss)	1mA	30nC	50nC		0.33	2	4	3	5	0.6	
DE275X2-102N06A		1000	48	750		6A	50uA (80% Vdss)	1mA	30nC	50nC		0.33	2	4	3	5	0.6	
IXFH12N100F (IXYS)		1000	48	300	TO-268 & TO-247	12A	50uA	1.5mA	42nC	77nC		0.42	10	12	12	31	0.8	
APT1201R2BLL	7	1200	48	400	TO-247	12A	100uA	500uA	59nC	99nC	391	0.31	9	21	14	44	11	
APT10078	7	100	56	400	TO-247	14A	100uA	500uA	59nC	93nC	429	0.31	8	9	9	30	7.87	
DE375-102N10A		1000	60	550		10A	50uA (80% Vdss)	1mA	40nC	90nC		0.23	3	5	5	8	0.6	
DE375-102N12A	**May-06**	**1000**	**72**	**550**		**12A**	**50uA (80% Vdss)**	**1mA**	**42nC**	**93nC**	**305**	**0.23**	**3**	**5**	**5**	**8**	**0.6**	**1.07**
APT12067xLL	7	1200	72	565	TO-264	18A	100uA	500uA	105nC	176nC	690	0.22	11	18	19	52	22	
APT12057	7	1200	88	690	TO-264 & TO-247	22A	100uA	500uA	126nC	211nC	830	0.18	12	21	21	58	25.5	
APT10045	7	1000	92	565	TO-264 & TMAX	23A	100uA	500uA	97nC	154nC	715	0.22	5	8	10	30	5.5	
DE475-102N20A		1000	120	600		20A	50uA (80% Vdss)	1mA	70nC	160nC		0.2	5	5	5	5	0.6	
DE475-102N21A	**May-06**	**1000**	**144**	**1800**		**21A**	**50uA (80% Vdss)**	**1mA**	**77nC**	**160nC**	**200**	**0.08**	**5**	**5**	**5**	**8**	**0.6**	**0.41**
APT12057B2FLL_LFLL	7	1200	88	690	TO-264	22A	250uA	1mA (80% Vdss)	120nC	185nC	770	0.18	20	21	11	36	18	0.57